ZnO-based metal-semiconductor field-effect transistors

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Referat:
Die vorliegende Arbeit befasst sich mit der Entwicklung, Herstellung und Untersuchung von ZnO-basierten Feldeffekttransistoren (FET). Dabei werden im ersten Teil Eigenschaften von ein- und mehrschichtigen Isolatoren mit hohen Dielektrizitätskonstanten betrachtet, die mittels gepulster Laserabscheidung (PLD) dargestellt wurden. Die elektrischen und kapazitiven Eigenschaften dieser Isolatoren innerhalb von Metall-Isolator-Metall (MIM) bzw. Metall-Isolator-Halbleiter (MIS) Übergängen wurden untersucht. Letzterer wurde schließlich als Gate-Struktur in Metall-Isolator-Halbleiter-FET (MISFET) mit unten (backgate) bzw. oben liegendem Gate (topgate) genutzt. Der zweite Teil konzentriert sich auf Metal-Halbleiter-FET (MESFET), die einen Schottky-Kontakt als Gate nutzen. Dieser wurde mittels reaktiver Kathodenzerstäubung (Sputtern) von Ag, Pt, Pd oder Au unter Einflußvon Sauerstoff hergestellt. ZnO-MESFET stellen eine vielversprechende Alternative zu den bisher in der Oxid-basierten Elektronik verwendeten MISFET dar. Durch die Variation des verwendeten Gate-Metalls, Dotierung, Dicke und Struktur des Kanals und Kontakstruktur, wurde ein Herstellungsstandard gefunden, der zu weiteren Untersuchungen herangezogen wurde. So wurde die Degradation der MESFET unter Belastung durch dauerhaft angelegte Spannung, Einfluss von Licht und erhöhten Temperaturen sowie lange Lagerung getestet. Weiterhin wurden ZnO-MESFET auf industriell genutztem Glasssubstrat hergestellt und untersucht, um die Möglichkeit einer großflächigen Anwendung in Anzeigeelementen aufzuzeigen. Einfache integrierte Schaltungen, wie Inverter und ein NOR-Gatter, wurden realisiert. Dazu wurden Inverter mit sogenannten Pegelschiebern verwendet, welche die Ausgangsspannung des Inverters so verschieben, dass eine logische Aneinanderreihung von Invertern möglich wird. Schließlich wurden volltransparente MESFET und Inverter, basierend auf neuartigen transparenten gleichrichtenden Kontakten demonstriert.

"We are stuck with technology when what we really want is just stuff that works."

– Douglas Adams, *The Salmon of Doubt* (2002)

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1 Introduction

The present thesis deals with the design, development and investigation of ZnO-based field-effect transistors (FET) for the use in future transparent electronics (TE). Transparent electronics have become a fast-growing field in semiconductor physics and material science due to its comprehensive applications in, e.g., transparent displays in windows and as transparent flat-panel TVs, invisible electronics in functional furniture or dishes, and augmented-reality devices. The key active devices for TE are transparent field-effect transistors (TFET), which are necessary as pixel-driver, for logic integrated circuits and memories. They are up to now mostly implemented as metal-insulator-semiconductor field-effect transistors (MISFET) consisting of a transparent semiconductor channel, a dielectric gate oxide and transparent contacts. As channel material, usually ZnO and ZnO-based amorphous oxides such as gallium indium zinc oxide (GIZO) or zinc tin oxide (ZTO) are used [1]. The gate dielectrics are usually oxides with high dielectric constants (high-κ) such as aluminium oxide, titanium oxide, zirconium oxide, hafnium oxide and mixed crystalls thereof. Indium tin oxide and degenerately doped ZnO:Al are used as transparent contacts.

The figures of merit for FET are: the ratio between the source-drain currents in the on- and in the off-state (on/off-ratio), the gate-voltage sweep needed for the given on/off-ratio, the channel mobility, and the subthreshold slope representing the logarithmic gain. For display applications, Wager recommended an on/off-ratio of $> 10^6$, a channel mobility $> 1\,\mathrm{cm}^2/\mathrm{Vs}$, and a device transmission of 70% [2]. For the implementation of TFET into integrated circuits (IC), a gate-voltage sweep $< 5\,\mathrm{V}$ and a subthreshold slope $< 200\,\mathrm{mV/decade}$ are additionally recommended [3].
Oxide MISFET and related IC usually suffer from high operating voltages due to the voltage drop across the insulator and limited switching speed due to the reduced channel mobility. The channel mobility of MISFET is reduced compared to the Hall-effect mobility of the used semiconductor due to scattering of carriers at the insulator/semiconductor interface [4]. Therefore, the issues for the fabrication of MISFET are the reduction of the insulator thickness and the reduction of interface defects under perpetuation of the insulating properties.

The main focus of this thesis is the realization of ZnO-thin-film-based metal-semiconductor field-effect transistors (MESFET) comprising a Schottky contact as gate. Due to the missing insulator and insulator/semiconductor interface, MESFET exhibit much lower operating voltages than MISFET and a higher channel mobility that ideally equals the semiconductor's Hall-effect mobility [5]. The MESFET presented in this thesis are a promising alternative approach to common MISFET based TE.

ZnO-thin-film MESFET were previously demonstrated by Ryu *et al.*, who used Ti as gate contact on p-type ZnO [6]. Kandasamy *et al.* used Pt-gate n-ZnO MESFET for hydrogen gas sensing [7]. Kao *et al.* used Pt/Au gate-contacts for their MESFET [8]. All reported thin-film ZnO MESFET show inferior electronic properties with high gate-voltage sweeps between 4 and 20 V, very low on/off-ratios below 1 decade and barely obtained pinch-off and saturation behavior in the output. On the basis

of ZnO nanorods, MESFET and logic devices such as OR, AND, NOT, and NOR-gates have been realized by Park *et al.* using Au-gate contacts [9]. Their on/off-ratio was $\sim 10^4$ and a subthreshold slope between 100 and 200 mV/decade was achieved. Channel mobilities were neither reported for ZnO thin-film nor nanorod MESFET.

2 Pulsed-laser-deposited metal-insulator-semiconductor field-effect transistors

For the reduction of MISFET operating voltages, high-κ insulators are needed. In this thesis, ZrO_2, HfO_2 as well as Al_2O_3–ZrO_2–Al_2O_3 and Al_2O_3–HfO_2–Al_2O_3 sandwich-layer insulators are grown by pulsed-laser deposition (PLD) and investigated by means of current-voltage (IV) and capacitance-voltage (CV) measurements within metal-insulator-metal (MIM) and metal-insulator-semiconductor (MIS) structures. The insulators grown at different substrate heater powers did not show a clear tendency. All insulators exhibit forward conduction for positive applied voltages at the Pt front-contact. Up to 80% of the contacts with ZrO_2 or HfO_2 are insulating for -1 V (leakage current density $< 2 \times 10^{-6}$ Acm^{-2}) but only 15% of the contacts are insulating at $+1$ V. For the sandwich-structure insulators, 80–100% (60–80%) of the contacts are insulating at -1 V ($+1$ V). The lower leakage currents can be explained by the higher band offset between Al_2O_3 and ZnO. The different material interfaces form a diffusion barrier for mobile ions. Temperature-dependent IV measurements reveal that the most probable mechanisms for the observed forward conduction are Schottky emission and Poole-Frenkel emission, indicating less importance of shunts and grain boundaries. The dielectric constants obtained from quasi-static CV measurements (QSCV) are in good agreement with the literature for the MIM structures and lay in the range between 13 for HfO_2 (13–16 [10]) and 25 for ZrO_2 (20–25 [11]). For the MIS diodes on ZnO, the highest κ-values are achieved for the highest substrate heater power and exceeded 33 for both HfO_2 and ZrO_2. QSCV measurements also reveal an excess of positive charges, i.e. metal, within the insulators, which may form defects that are responsible for the observed forward conduction. The amount of these charges is found to be a factor of 10 to 20 lower for sandwich insulators than for single-layer insulators.

A top-gate ZnO-MISFET with a 90 nm thick Al_2O_3–HfO_2–Al_2O_3 sandwich-insulator is fabricated [12]. Its transfer characteristic is compared with a typical ZnO-MESFET on sapphire in Fig. 1a. The normally-on MISFET exhibits a turn-on voltage of -6 V and the source-drain current can be tuned over five orders of magnitude within a gate-voltage sweep of only 7 V. The minimum subthreshold slope of 300 mV/decade is among the best reported ZnO-MISFET. However, the channel mobility of 1.9 cm^2/Vs is a factor of ten lower than the Hall-effect mobility, which can be attributed to scattering at interface-trap charges. The interface-trap charge density was measured by admittance spectroscopy and lay in the range of 10^{11}–10^{12} cm^{-2}eV^{-1}, which is similar to other reported values for these insulators [13].

For the bottom-gate ZnO MISFET, a more than 800 nm thick Al_2O_3 layer is necessary to reduce the leakage currents below 10^{-10} A at ± 60 V. A comparison is made between *a*-plane and *r*-plane sapphire substrates. Both MISFET show normally-on behavior with turn-on voltages between -40 and -50 V. The on-current, on/off-ratio and channel mobility is higher for the *r*-plane MISFET due to its higher free-carrier concentration. Here, the diffusion of donors in to the ZnO-channel seems to be more likely. Compared to the top-gate MISFET, the channel mobilities of the bottom-gate MISFET are significantly lower (0.3 cm^2/Vs and 0.5 cm^2/Vs for *a*-plane and for *r*-plane sapphire, respectively). Similar channel mobilities were also observed for a bottom-gate MISFET using an equally grown ZnO channel and a ferroelectric $BaTiO_3$-insulator on $SrTiO_3$ substrate [14].

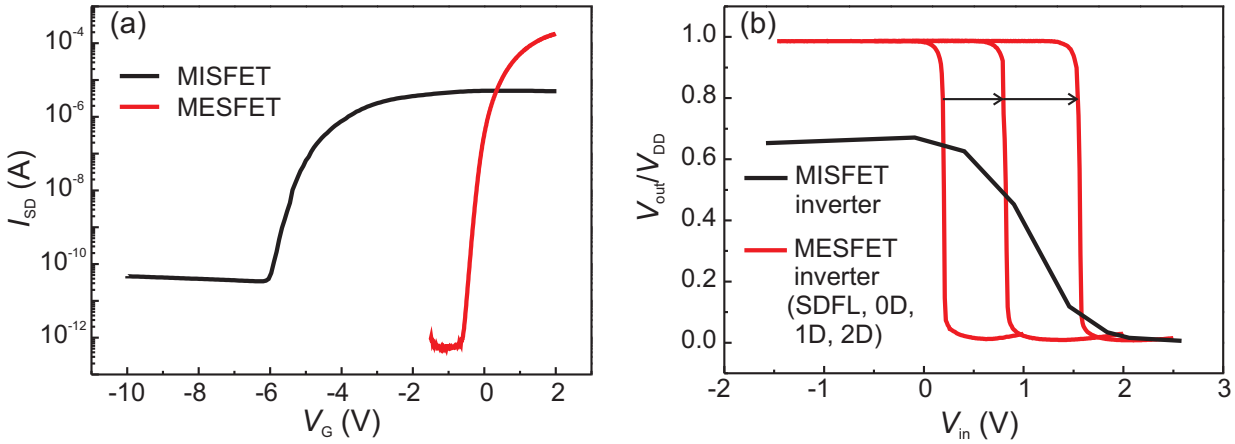

Figure 1: a) Transfer characteristics of the best MISFET realized within this thesis and a typical MESFET with $W/L = 21.5$. b) Voltage-transfer characteristics of a MISFET-based inverter from [23] and a MESFET-SDFL inverter of this thesis with zero, one and two Schottky diodes as level-shifter.

3 ZnO-based metal-semiconductor field-effect transistors

ZnO-based MESFET are fabricated using highly rectifying Schottky contacts deposited by means of reactive dc-sputtering of Ag, Pt, Pd or Au on thin ZnO channels. It has been shown by Lajn *et al.*, that, except of Au, the metals are partially oxidized on ZnO thin films [15]. The dominant transport mechanism is similar to metallic Schottky contacts thermionic emission and their Schottky barrier heights are increased compared to pure metals. For reactively sputtered Schottky contacts on ZnO single-crystals, this has been reported by Allen *et al.* [16, 17]. For the MESFET-gate diodes, the Schottky barrier heights are as high as 0.95 V, 0.90 V, 0.79 V and 0.69 V for Ag, Pt, Pd and Au, respectively [18]. For thin films on sapphire substrate, all possible design parameters for ZnO-MESFET are varied: gate material, channel thickness and doping, gate geometry as well as channel mobility [19]. A standard configuration is found using Ag_xO as gate on a nominally undoped, 20 to 30 nm thick ZnO channel without buffer layer. With that, an on/off-ratio of 10^8 and a channel mobility $> 10\,cm^2/Vs$ is achieved within a gate-voltage sweep of only 3 V. [5]. The minimum slope of ~ 80 mV/decade is already close to the thermodynamic limit of 60 mV/decade for FET operating at room-temperature. The highest channel mobility for the standard configuration is $27\,cm^2/Vs$. It is shown that the channel mobility of the ZnO-MESFET is usually equal to the respective Hall-mobility, which is the major advantage of MESFET compared to MISFET. However, leakage currents may lead to the underestimation of the channel mobility.

MESFET with Ag_xO and PtO_x gates show similar electrical performances. Ag_xO is used as standard, because the MESFET exhibited lower leakage currents and higher stability at elevated temperatures. By means of a MgO-buffer layer between sapphire substrate and a nominally undoped ZnO-channel, the net doping concentration in the channel is reduced from $\sim 10^{18}\,cm^{-3}$ to $10^{14}\,cm^{-3}$ due to the reduced diffusion of Al from the sapphire. Based on that, it is possible to intentionally dope the channel. A reduced doping concentration leads to a reduced scattering on charged impurities. However, the variation of the Al-content in ZnO-targets between 0.001 wt-% and 1 wt-% led again to doping concentrations in the high $10^{18}\,cm^{-3}$-range and excessive leakage currents. Increasing the thickness of the undoped ZnO-channel to ~ 120 nm on MgO-buffer results in a decreased on/off-ratio of $\sim 10^4$ compared to the standard configuration due to the lower on-current. The highest on-current of 15 mA and on/off ratio of 5×10^8 is achieved using an interdigitated contact geometry with a gate width-to-length-ratio of 700 making the MESFET suitable for applications as pixel-driver transistors for active-matrix LCD or OLED displays [20]. An increase of the MESFET channel mobility up to $50\,cm^2/Vs$ is achieved by the improvement of the channel crystal quality using homoepitaxially grown ZnO [12]. However, these MESFET have shown insufficient saturation behavior due to parasitic

currents through the ZnO substrate and their channel mobility is underestimated by a factor of three compared to the Hall-effect mobility. A further way to increase the channel mobility is demonstrated using a quantum-well (QW) structure. The formation of a two-dimensional electron gas in the MgZnO/ZnO/MgZnO-QW is observed at a gate voltage of 0.5 V. In the same voltage range, a peak-like increase of the channel transconductance is observed, which is directly related to the channel mobility.

Reliability and degradation effects of the MESFET are investigated at elevated temperatures, under the exposure to visible light, by means of bias stress and long-term stability measurements. The MESFET with Ag_xO and PtO_x gates are stable until temperatures of 100°C and 75°C, respectively, without showing a significant increase in off-current or turn-on-voltage shift [18]. Temperatures above these values result in irreversible degradation of the MESFET. Bias stress measurements on the MESFET reveal no influence of interface charges, i.e. under positive or negative gate-voltage stress over a period of 22 hours, no turn-on voltage shift is observed, which represents a major advantage of MESFET compared to MISFET. An influence of visible light on the off-current and the turn-on voltage is observed for blue and violet light. The maximum turn-on voltage shift under irradiation of violet light is 0.65 V compared to shifts between 2 V and 20 V for amorphous-channel MISFET [21].

Long-term stability measurements show a decrease of the channel mobility and on/off-ratio for the ZnO-channel MESFET after 100 days before they stay constant [19]. Using ZnO-channels with a small amount (0.25%) of Mg leads to lower initial values that are, however, constant for the whole periode of 300 days. It is further observed that the reproducibility of the MgZnO-MESFET is higher than for ZnO-MESFET.

ZnO-MESFET are fabricated on industrially more relevant glass substrates. For that, a ZnO target with 0.01 wt-% Al and an oxygen partial pressure of 3×10^{-4} mbar is used aberrant from the standard configuration for sapphire substrate. A comparison of MESFET on quartz glass and on two commercial borosilicate substrates show a significant difference in the channel conductivity [22]. All MESFET on glass are normally-off due to compensation by indiffusion of elements such as Li, Na, K, B from the substrate into the channel. A broad distribution of defects is observed by means of admittance spectroscopy. The highest channel mobility of $1.3\,cm^2/Vs$ and on/off-ratio of 4.7×10^5 is achieved for quartz. The MESFET on borosilicates exhibit one and two decades lower channel mobilities. Contrary to the MESFET on sapphire, a fast degradation of the electrical properties for MESFET on quartz glass is observed already within a periode of 10 days. The turn-on voltage, on/off-ratio and channel mobility decrease, whereas the Ag_xO-gate Schottky barrier height increases. This implies an alteration of the oxidation of the gate material. During bias stress measurements, a small turn-on voltage shift of 0.2 V is observed under dark conditions, which is, however, assigned to the reduction of an initially photogenerated charge at the gate/channel interface. Under permanent illumination, those charges are not observed.

4 Inverter

Based on ZnO-MESFET technology developed within this thesis, integrated logic circuits are fabricated. Three types of inverters: simple inverter, FET-logic (FL) inverter and Schottky-diode FET-logic (SDFL) inverter are investigated. With the simple inverter, consisting of two normally-on MESFET, the peak gain magnitude can be tuned in the range between 2.5 at an operating voltage of 1 V and 250 at 4 V; the uncertainty level stays constant at ~ 0.3 V. These values are superior to comparable ZnO-MISFET inverters [23] (cf. Fig. 1b). Deviations of the real inverter characteristics from the ideal one are related to leakage and breakdown currents of the switching transistor for the high-output and low-output deviation, respectively. The positive switching-point deviation is assigned to charge trapping at the gate/channel-interface.

The principle of a level shifter consisting of Schottky diodes and an additional MESFET at the

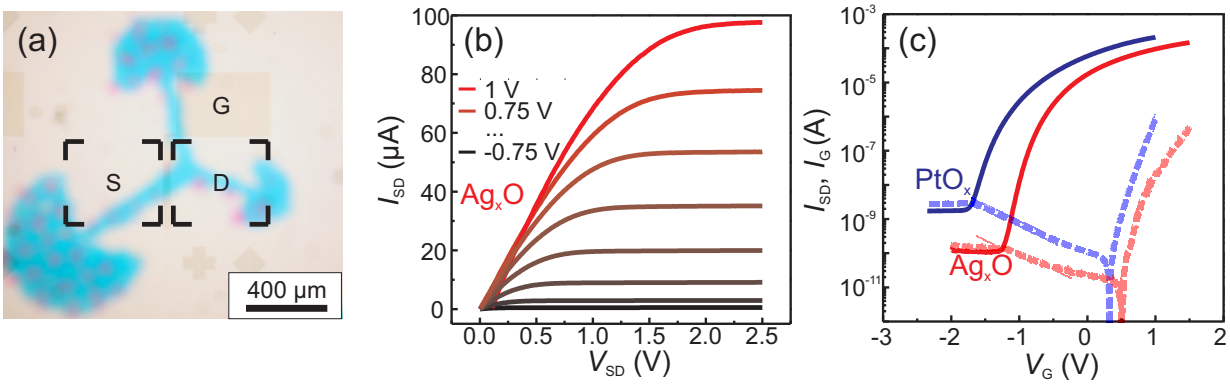

Figure 2: a) Microscopic image of a transparent MESFET, Background: printed logo of the graduate school "BuildMoNa" on a transparency. b) Output characteristics of a transparent MESFET with Ag_xO. c) Transfer and gate characteristics of transparent MESFET with Ag_xO and PtO_x.

output side (FL) or input side of the inverter (SDFL) is demonstrated for the ZnO-MESFET inverters. This is adapted from commonly known GaAs MESFET technology [24]. For the FL-inverter, the output-voltage is shifted up to $-1.2\,V$ at a pull-down voltage of $-1.5\,V$. The uncertainty level is reduced to $\sim 0.1\,V$, which is similar to GaAs inverters. Using the SDFL-inverter, the influence of the switching transistor turn-on voltage on the voltage-transfer curve is investigated [25]. For the lower negative turn-on voltage of the switching transistor, the inverter achieves a higher peak gain magnitude of 197 and the lower uncertainty level of 0.13 V at 3 V operating voltage, whereas it is only 141 and 0.37 V, respectively, for the higher negative turn-on voltage. The input-voltage is shifted by 1.5 V with two additional Schottky diodes. Connecting a third diode at the input of the inverter, a NOR-gate is implemented.

5 Transparent rectifying contacts

For the realization of fully transparent ZnO-MESFET electronics, transparent rectifying contacts (TRC) are developed and demonstrated within Schottky diodes, MESFET and inverters [3]. A patent application has been filed [26]. The contacts consist of the ZnO-channel layer, an ultrathin ($\sim 5\,nm$) transparent Ag_xO or PtO_x layer and an equally thin highly conductive oxide or metal as capping layer. The overall transmission of the complete device structure is 70% and 60% for Ag_xO and PtO_x, respectively. The Schottky diodes show excellent rectifying behavior with an ideality factor of only 1.47, a maximum barrier height of 0.87 V and the reverse leakage currents at -2V were as low as $10^{-6}\,A/cm^2$. The fully transparent MESFET and inverters exhibit similar electrical properties as the presented opaque devices. With an on/off-ratio of 1.4×10^6, a channel mobility of $12\,cm^2/Vs$ and a maximum gate-voltage sweep of 3 V, (Fig. 2) as well as a peak gain magnitude of ~ 200 and an uncertainty level of 0.36 V for the MESFET and the inverters, respectively, the devices are among the best reported transparent transistors or inverters of any kind.

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1 Introduction

Transparent electronics (TE) have become an emerging field of material science and semiconductor physics in the past decade [Wag03]. It provides the vision of numerous applications and designs, such as transparent displays in the windshields of cars and planes, large-area displays in windows or as transparent flat-panel TVs. Furthermore, surfaces of products can be functionalized, e.g. realizing furniture or dishes with invisible electronics. And, using transparent displays, augmented-reality devices can be designed, which provide additional information to the seen objects, e.g. for aircraft mechanics, surgeons or tourists.

For that, transparent wide band gap materials, such as nitrides, carbides, diamond and oxides, with well-controlled electronic properties are necessary. From these materials, the group of oxides exhibit the highest variety of electronic properties. For oxides, the two extremes of the conductivity range are most developed and established in today's electronic industry. On the one hand, wide-bandgap ceramic oxides such as Al_2O_3, ZrO_2/HfO_2, and TiO_2 are introduced as highly insulating materials with high dielectric constants (high-κ) [Rob06] for the use in capacitors or as gate oxide in metal-insulator-semiconductor field-effect transistors (MISFET) replacing silicon oxide in microelectronics. On the other hand, degenerately doped ($n \sim 10^{21}\,\mathrm{cm}^{-3}$) oxides (transparent conducting oxides, TCO), foremost indium tin oxide (ITO) or Al-doped ZnO (AZO), are widely used as highly conductive transparent front contacts to various devices such as liquid-crystal displays, solar cells and touch screens [Min05]. Materials having intermediate conductivities with carrier concentrations in the range of 10^{14}–$10^{18}\,\mathrm{cm}^{-3}$ are referred to as transparent semiconducting oxides (TSO) [Gru10]. Their conductivity can be controlled via the manipulation of a depletion layer by a gate-electrode potential.

Using TSO, transparent field-effect transistors (TFET), necessary as pixel-driver for displays as well as for logic integrated circuits (IC) and memories, are developed as key active devices for TE. They are up to now mostly implemented as MISFET based on ZnO and related oxides.

However, such MISFET and related IC usually suffer from higher operating voltages due to the voltage drop across the insulator and limited switching speed due to carrier scattering at the interface between insulator and semiconductor. The channel mobility of MISFET is reduced compared to the bulk mobility of the semiconductor [Zeg04] resulting in lower gain. Due to the missing insulator and insulator/semiconductor interface, MESFET exhibit higher gain with lower operating voltages and the channel mobility equals the bulk mobility. They can further be fabricated more cost-efficiently.

The first completely transparent, i.e. substrate, channel, gate and contacts, TFET was fabricated by R. L. Hoffman *et al.* in 2003 [Hof03]. This MISFET comprises a ZnO channel, aluminium titanium oxide as gate dielectric and ITO as gate, source and drain contacts. Besides ZnO, which strongly tends to grow polycrystalline, the state of technology for MISFET also comprises amorphous-oxide channels, e.g. gallium indium zinc oxide or zinc tin oxide [Lee09b, Gö06], on glass substrates. Those devices exhibit channel mobilities in the range of $10\,\mathrm{cm}^2/\mathrm{Vs}$ and on/off-ratios $> 10^7$.

Metal-semiconductor field-effect transistors (MESFET) are commonly known from GaAs-technology [Sed04] and are used for high-speed logic circuits due to their large channel mobility [Miz80, Tuy74]. For ZnO, MESFET technology was previously demonstrated by Ryu *et al.*, who used Ti as gate contact on *p*-type ZnO [Ryu05]. Kandasamy *et al.* used Pt-gate *n*-ZnO MESFET for hydrogen gas sensing [Kan07a]. Kao *et al.* used Pt/Au gate-contacts for their MESFET [Kao05]. However, the reported thin-film ZnO MESFET show inferior electronic properties with high gate-voltages between 4 and 20 V, very low on/off-ratios below 1 decade and barely obtained pinch-off and saturation behavior. On the basis of ZnO nanorods, MESFET and logic devices such as OR, AND, NOT, and NOR-gates have been realized by Park *et al.* using Au-gate contacts [Par05]. Their on/off ratio was $\sim 10^4$ and a subthreshold slope between 100 and 200 mV/decade was achieved. Channel mobilities were neither reported for ZnO thin-film nor nanorod MESFET.

The goal of the present thesis is to realize and compare properties of ZnO thin-film-based FET (MISFET and MESFET) and to design, develop and investigate MESFET as an alternative approach to MISFET devices for the use in transparent circuitry. Design parameters shall be identified and the reliability of ZnO-MESFET is investigated.

This thesis is embedded in the German Research Foundation within the Collaborative Research Centre SFB 762: "Functionality of Oxide Interfaces". All investigated samples were fabricated and processed in the Semiconductor Physics Group at Universität Leipzig. Structural, morphologic, and electrical characterizations were also performed in this group.

Preliminary to the fabrication of MESFET, PLD-grown high-κ insulators and their application in MISFET are investigated in order to gain a basic understanding of the problems that are related to the insulator. For that, the conductive and capacitive properties of various insulators were studied in metal-insulator-metal (MIM) structures and the most promising dielectrics are then considered for metal-insulator-semiconductor (MIS) diodes on ZnO to electrically inquire the formation of defects at the insulator/semiconductor interface. Finally, MISFET were fabricated and analyzed.

MESFET were designed and fabricated on the basis of reactively dc-sputtered highly-rectifying Schottky contacts on ZnO [Laj09]. Based on a first-prinicples MESFET model [Sze81, Zeg04], physical parameters of MESFET such as channel thickness, doping and mobility as well as gate metals and contact design were varied and their influence on the performance of MESFET on sapphire substrate was investigated. The MESFET technology was then transferred to various low-cost glass substrates to prove their industrial applicability. For both kind of substrates, reliability tests were performed considering the degradation under bias stress, exposure to visible light and long-time stability. The properties of the MESFET were compared to MISFET within this work and and other reported MISFET.

Emanating from the findings on MESFET, three types of inverter circuits and a NOR-gate were realized. Their electrical performance as well as deviations from the ideal case were investigated.

Finally, a layer structure and preparation method for transparent rectifying contacts (TRC) wass developed. The TRC serve as basis of fully-transparent Schottky-diodes, MESFET and inverters for applications in transparent electronics. Transparent MESFET and inverters were compared to other reported transparent devices and the opaque devices presented in this work.

The pulsed-laser deposition (PLD) of the samples was carried out by Dipl.-Ing. H. Hochmuth, photolithography and processing was done in collaboration with Dipl.-Ing. G. Biehne and M. Hahn,

dc-sputtering of the contact metalls was performed in collaboration with H. Münch. The pre-characterization of the FET samples with spectroscopic ellipsometry was done by the Ellipsometry Workgroup (Dipl.-Phys. C. Sturm, Dipl.-Phys. H. Hilmer, Dr. R. Schmidt-Grund, *et al.*), Hall-effect measurements were performed by Dipl.-Phys. M. Brandt, Dipl.-Phys. R. Heinhold and Dipl.-Phys. T. Lüder. SEM cross-sections and EDX-analysis were carried out by Dipl.-Phys. J. Lenzner, TEM was performed by Dr. G. Wagner. XRD and AFM was measured by Dipl.-Phys. M. Lorenz, AFM was also measured by Dipl.-Phys. M. Brandt and Dipl.-Phys. G. Zimmermann. Electrical measurements on MESFET on glass substrates, inverters and MIM/MIS-capacitors were performed in collaboration with Dipl.-Phys. M. Lorenz, Dipl.-Phys. F. Schein and M.Sc. N. Yensuong, respectively, within the scope of their diploma and master thesises. The electrical characterization of transparent devices was done in collaboration with Dipl.-Phys. A. Lajn and T. Diez. Chemical analysis by means of TOF-SIMS measurements was performed by S. Richter (Fraunhofer CSP, Halle).

2 Basics of field-effect transistors and integrated circuits

Field-effect transistors are unipolar transistors where only one type of charge carriers (either electrons or holes) are involved in the current transport. This thesis mainly focuses on MESFET and MISFET whose gate structure is a metal-semiconductor junction (Schottky diode) or a metal-insulator-semiconductor junction (MIS diode), respectively. The physical basics of these structures shall be the topic of this chapter. At the end of this chapter, the basics of integrated logic circuits, that were realized within this work, will be presented.

2.1 Metal-semiconductor junction

First metal-semiconductor junctions on ZnO were investigated by C. A. Mead in 1965 [Mea65]. The formation of such a junction on any *n*-type semiconductors can be described by the model developed in 1939 by W. Schottky [Sch39] and N. F. Mott [Mot39]. It is therefore called Schottky-Mott diode or Schottky contact. The rectifying partially oxidized gate contacts within this thesis can be well treated by this model. It will be shown in Cha. 5, that metall-oxide Schottky contacts on ZnO thin films exhibit a higher barrier height than pure metallic Schottky contacts.

2.1.1 Band diagram

Within the Schottky-Mott model, a Schottky contact is obtained in the case:

$$\phi_\mathrm{m} > \chi_\mathrm{s} + \phi_\mathrm{n} \,, \tag{2.1}$$

where ϕ_m is the metal's work function, χ_s is the electron affinity of the semiconductor and $\phi_\mathrm{n} = E_\mathrm{C} - E_\mathrm{F}$ is the energy difference between conduction band edge E_C and Fermi energy level E_F. The formation of a Schottky contact is illustrated in the band diagram of Fig. 2.1. When both materials are brought in ideal contact and surface states and interface roughness are neglected, electrons from the semiconductor will move to the energetically more favorable states in the metal. A current flows until the Fermi levels of both sides are equal. The electrons were provided by donors in the semiconductor, whose positively charged cores form a space charge region in the vicinity of the metal-semiconductor interface. A potential barrier ϕ_B is formed due to charge neutrality and the subsequent band bending in the semiconductor. The Schottky barrier height is given by [Sze81]:

$$\phi_\mathrm{B} = \phi_\mathrm{m} + \chi_\mathrm{s} \,. \tag{2.2}$$

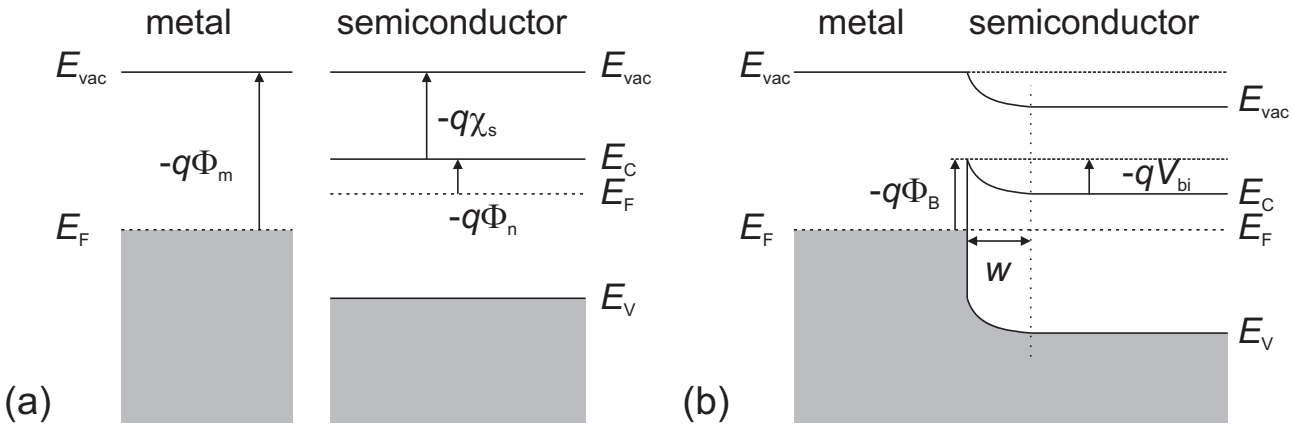


Figure 2.1: Band diagrams of a Schottky metal and a *n*-type semiconductor a) before contact and b) after formation of the Schottky contact.

Table 2.1: Work function ϕ_m and Schottky barrier height ϕ_B for various pure metals assuming an electron affinity for ZnO of χ_s = 4.1 eV [Nak07, Jac84].

	$q\phi_m$ (eV)	$q\phi_B$ (eV)
Pt	5.65	1.55
Pd	5.12	1.02
Au	5.10	1.10
Ag	4.26	0.16

It is in first principles independent of the doping or applied external voltages. In the semiconductor, the built-in voltage $V_{bi} = \phi_m - (\chi_s + \phi_n)$ drops over the width w of the space charge region. A space charge region is also formed in the metal. However, due to the very high electron density and screening effects, it is only a few angstroms wide. Table 2.1 lists the work function and Schottky barrier height on ZnO for the pure metals, that were reactively sputtered in this work. Note, that Ag/ZnO would result in very low Schottky barrier height and would lead to an ohmic contact. Ag_xO, however, leads to much higher ϕ_B as will be shown in Sec. 5.1. The electron affinity of ZnO is thereby assumed to be χ_s = 4.1 eV [Nak07]. However, Jacobi *et al.* showed, that χ_s is higher for the oxygen terminated surface than for the zinc terminated surface [Jac84]. Since, for the very thin ZnO films used as channel in this thesis, the surface termination is not clear, the average χ_s of both surfaces (4.1 eV) is assumed.

2.1.2 Capacitance-voltage characteristic

The space charge region underneath a Schottky contact can be considered as a plate capacitor with the capacitance per unit area

$$C = \frac{\epsilon_r \epsilon_0}{w} = \frac{Q}{V}\,, \tag{2.3}$$

where ϵ_r and ϵ_0 are the dielectric constant of the semiconductor and the vacuum dielectric constant, respectively. Q is the charge that was measured at a given voltage V. The space charge region width w can be determined making the assumption that the space charge is given by the net doping concentration: $\rho = q(N_D - N_A)$. Within the Schottky approximation, no charge and no electric field shall be outside of the space charge region, i.e. $\rho = 0$ and $\mathcal{E} = \partial V/\partial x = 0$.Then, the one dimensional Poisson equation

$$\Delta_x V = -\frac{\rho}{\epsilon_r \epsilon_0} \tag{2.4}$$

can be solved with the ansatz $V = V_0 + V_1 x + V_2 x^2$ and the boundary condition $V(0) = -V_{bi}$. Double integration results in the potential:

$$V(x) = -V_{bi} + \frac{q(N_D - N_A)}{\epsilon_r \epsilon_0}\left(wx - \frac{1}{2}x^2\right) . \tag{2.5}$$

Due to the finite width of the space charge region ($V(w) = 0$), w can be extrated from Eqn. 2.5:

$$w = \sqrt{\frac{2\epsilon_r \epsilon_0}{q(N_D - N_A)} V_{bi}} . \tag{2.6}$$

Applying a positive external voltage V_{ext} and considering the thermal energetic broadening of electrons $k_B T/q$ reduces w:

$$w = \sqrt{\frac{2\epsilon_r \epsilon_0}{q(N_D - N_A)}\left(V_{bi} - V_{ext} - \frac{k_B T}{q}\right)} . \tag{2.7}$$

From Eqns. 2.3 and 2.7, the net doping concentration can be calculated from the slope of C^{-2}(V):

$$N_D - N_A = -\frac{2}{q\epsilon_r \epsilon_0}\left(\frac{\partial C^{-2}}{\partial V}\right)^{-1} . \tag{2.8}$$

Within this work, the determination of the net doping concentration is done by means of quasi-static capacitance-voltage measurements as described in Sec. 3.5.

2.1.3 Current-voltage characteristic

The principle conduction mechanisms for *n*-type Schottky diodes are:

1. Thermionic emission of electrons above the barrier.
2. Tunneling of electrons through a thin barrier; e.g. for highly doped semiconductors.
3. Recombination within the space charge region.

4. Injection of holes from the metal and subsequent recombination outside of the space charge region.

For moderately doped semiconductors, thermionic emission is the predominant mechanism. The Schottky-diode characteristics within this thesis are treated by thermionic emission theory. Its derivation is based on the descriptions in [Sze81] and [Gru06].

The emission of electrons from the semiconductor to the metal above the barrier is given by

$$j_{\mathrm{sm}} = -\int q v_{\mathrm{x}} dn \,, \tag{2.9}$$

where dn is the electron density in a small energy intervall given by the density of states $D(E)$ and the Fermi distribution $f(E)$. For a bulk semiconductor and using the Boltzmann approximation, dn is:

$$dn = D(E) f(E) dE = \frac{4\pi (2m^*)^{3/2}}{h^3} \sqrt{E - E_{\mathrm{C}}} \cdot \exp\left(\frac{E - E_{\mathrm{F}}}{k_{\mathrm{B}} T}\right) dE \,. \tag{2.10}$$

Using the substitutions

$$E - E_{\mathrm{C}} = \frac{m^*}{2} v^2 \tag{2.11}$$

$$dE = m^* v dv = 4\pi v^2 dv_{\mathrm{x}} dv_{\mathrm{y}} dv_{\mathrm{z}} \tag{2.12}$$

$$E - E_{\mathrm{F}} = E - E_{\mathrm{C}} + q(\phi_{\mathrm{B}} + V_{\mathrm{bi}}), \tag{2.13}$$

Eqn. 2.10 can be re-written as:

$$dn = 2\left(\frac{m^*}{h}\right)^3 \exp\left(\frac{q(\phi_{\mathrm{B}} + V_{\mathrm{bi}})}{k_{\mathrm{B}} T}\right) \exp\left(\frac{\frac{m^*}{2} v^2}{k_{\mathrm{B}} T}\right) dv_{\mathrm{x}} dv_{\mathrm{y}} dv_{\mathrm{z}} \,. \tag{2.14}$$

With that, the integral in Eqn. 2.9 can be solved and the current density results in

$$j_{\mathrm{sm}} = A^* T^2 \exp\left(\frac{q\phi_{\mathrm{B}}}{k_{\mathrm{B}} T}\right) \exp\left(\frac{qV}{k_{\mathrm{B}} T}\right) \,, \tag{2.15}$$

where V is the external applied voltage and $A^* = \frac{4\pi q m^* k_{\mathrm{B}}^2}{h^3}$ is the Richardson constant, which is $A^* = 32.4 \, \frac{\mathrm{A}}{\mathrm{cm^2 K^2}}$ for ZnO.

With zero net current for $V = 0$ in thermal equilibrium, the current from the metal to the semiconductor can be extracted from Eqn. 2.15:

$$j_{\mathrm{ms}} = -A^* T^2 \exp\left(\frac{q\phi_{\mathrm{B}}}{k_{\mathrm{B}} T}\right) \,. \tag{2.16}$$

Thus, the current-voltage characteristic of the Schottky diode is given by

$$j = \underbrace{A^* T^2 \exp\left(\frac{q\phi_\mathrm{B}}{k_\mathrm{B}T}\right)}_{j_\mathrm{s}} \left[\exp\left(\frac{qV}{k_\mathrm{B}T}\right) - 1\right] , \tag{2.17}$$

with j_s being the saturation current density. If the Schottky effect, i.e. the change of barrier height with bias voltage, is considered, the ideality factor

$$\eta = 1 + \frac{\partial \phi_\mathrm{B}}{\partial V} \tag{2.18}$$

has to be introduced. The ideality factor should be close to unity $\eta \leq 1.03$ if the voltage dependence of the barrier height is only due to image force lowering. However, the real values are higher , which is most probably due to an inhomogeneous barrier height [Wer91].

2.2 Metal-insulator-semiconductor junction

2.2.1 Band diagram

In this section, the ideal MIS diode is considered, i.e. under an applied external voltage, charges only exist either at the metal-insulator interface or, with opposing charges, in the semiconductor — no charges are allowed within the insulator. The case of a non-ideal insulator is discussed in Sec. 3.4.2. The insulator is ideal, when its resistivity is infinite. It also implies the absence of charges at the insulator-semiconductor interface (the opposite case is discussed in Sec. 3.5). At zero external voltage, there is no difference between the metal's and the semiconductor's work functions:

$$\phi_\mathrm{ms} = \phi_\mathrm{m} - \phi_\mathrm{s} = \phi_\mathrm{m} - \left(\chi_\mathrm{s} + \frac{E_\mathrm{g}}{2q} - \psi_\mathrm{B}\right) = 0 , \tag{2.19}$$

where ϕ_m and ϕ_s are the work functions of the metal and the semiconductor, respectively, χ_s is the electron affinity of the semiconductor, E_g the band gap, q the elementary charge and ψ_B the difference between Fermi energy level E_F and the intrinsic energy level E_i. The definitions of the potentials are shown within the band diagram (Fig. 2.2) of an ideal MIS diode for flat-band condition (Eqn. 2.19).

For n-type semiconductors, ψ_B can be obtained from the bulk electron concentration

$$n \approx N_\mathrm{D} = n_\mathrm{i} e^{(E_\mathrm{i} - E_\mathrm{F})/k_\mathrm{B}T} , \tag{2.20}$$

where n_i is the intrinsic carrier concentration, N_D the donor concentration. Therefore, ψ_B can be obtained as

$$\psi_\mathrm{B} = \frac{k_\mathrm{B}T}{q} \ln \frac{N_\mathrm{D}}{n_\mathrm{i}} . \tag{2.21}$$

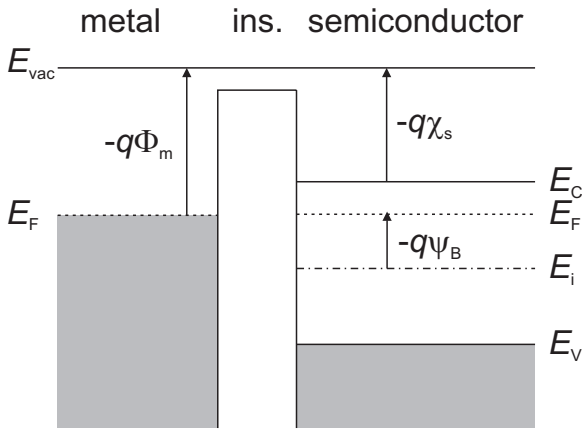


Figure 2.2: Band diagram of an ideal MIS diode in flat-band condition (no external voltage applied).

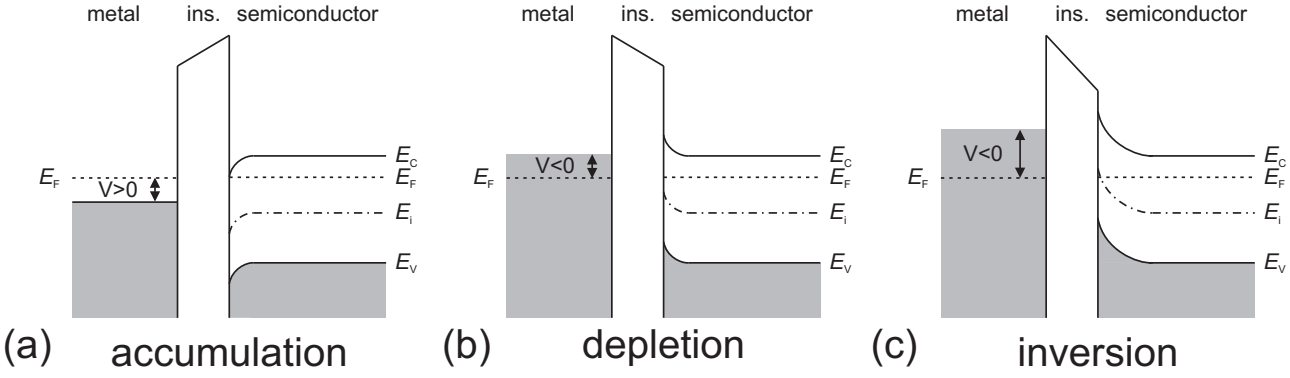


Figure 2.3: Band diagrams of an ideal MIS-diode with applied external voltage: a) accumulation ($V > 0$), b) depletion ($V < 0$) and c) inversion ($V \ll 0$).

When an external voltage is applied to the MIS structure, three cases are possible (Fig. 2.3): a) accumulation, b) depletion and c) inversion. To explain these cases, the potential ψ is defined as the difference between the intrinsic energy level in the bulk of the semiconductor and at a given position x:

$$\psi(x) = -\frac{E_i(x) - E_i(\infty)}{q} \,. \tag{2.22}$$

The potential is zero in the bulk and defined as surface potential ψ_s for $x = 0$.

a) Accumulation

If the applied voltage is positive on the metal side of the junction, the bands are bent downward with respect to the Fermi energy level, as no current flow is allowed through the ideal insulator (Fig. 2.3a). The surface potential ψ_s is positive. Due to charge neutrality, the positive charges at the metal gate are equalized by an accumulation of electrons at the semiconductor surface ("field-effect").

b) Depletion

The band is bent upwards as negative voltage is applied at the metal. The surface potential ψ_s is now negative but does not exceed ψ_B, i.e. E_i does not cross E_F. A depletion layer is formed, similar to the case of a Schottky contact, which expands as the voltage is increased in the negative direction.

C) Inversion

When the negative voltage is further increased above ψ_B, E_i crosses E_F. Thermal generation of holes becomes more and more probable. The hole density at the surface is then larger than the electron density. An inversion layer is formed at the surface. For ZnO, inversion due to thermal generation of holes cannot be observed because of the large band gap as discussed in Sec 2.2.2.

2.2.2 Capacitance-voltage characteristic

In order to derive a model for the capacitance-voltage (CV) characteristic of a MIS diode, a relationship between the surface charge Q_s, surface electric field $\mathcal{E}_s$ and surface potential ψ_s is required. The following derivation is based on [Sze81] for an *n*-type semiconductor.

The relation between the potential ψ and the densities of holes and electrons in the semiconductor is given by

$$n_n(x) = n_{n_0} \exp\left(\frac{q\psi(x)}{k_B T}\right) , \tag{2.23}$$

$$p_n(x) = p_{n_0} \exp\left(\frac{-q\psi(x)}{k_B T}\right) , \tag{2.24}$$

where n_{n_0} and p_{n_0} are the densities of electrons and holes at equilibrium, respectively. Therefore, the surface density for electrons and holes at $x = 0$ can be obtained for $\psi(0) = \psi_s$:

$$n_s = n_{n_0} \exp\left(\frac{q\psi_s}{k_B T}\right) , \tag{2.25}$$

$$p_s = p_{n_0} \exp\left(\frac{-q\psi_s}{k_B T}\right) . \tag{2.26}$$

In order to obtain the function $\psi(x)$, the one dimensional Poisson equation (Eqn. 2.4) has to be solved with the total space charge

$$\rho(x) = q(N_D - N_A + p_n(x) - n_n(x)) . \tag{2.27}$$

Since far from the surface, charge neutrality has to be considered with $\psi(\infty) = 0$ and $\rho(x) = 0$, it can be seen that $n_{n_0} - p_{n_0} = N_D - N_A$. With the thermal potential $\phi_t = k_B T/q$ and the permittivity of the semiconductor $\epsilon_s = \epsilon_r \epsilon_0$, the Poisson equation can be written as

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{q}{\epsilon_s}\left[p_{n_0}\left(\exp\left(-\frac{\psi(x)}{\phi_t}\right) - 1\right) - n_{n_0}\left(\exp\left(\frac{\psi(x)}{\phi_t}\right) - 1\right)\right] . \tag{2.28}$$

This equation is then multiplied from both sides with $2(\partial\psi/\partial x)$ such that the left side becomes $(\partial/\partial x)(\partial\psi/\partial x)^2$. Integration from the bulk toward the surface with $\mathcal{E} = -\partial\psi/\partial x$ being the electric field leads to

$$\mathcal{E} = \pm\frac{\sqrt{2}\phi_t}{L_D}\mathcal{F}(\psi) . \tag{2.29}$$

For $\psi > 0$, the sign is negative and for $\psi < 0$ it is positive. The notation of $\mathcal{F}(\psi)$ and the extrinsic Debye length L_D, with $\frac{p_{n_0}}{n_{n_0}} = \frac{n_i^2}{N_D^2}$, is:

$$\mathcal{F}(\psi) = \left[\frac{n_i^2}{N_D^2}\left(\exp\left(-\frac{\psi}{\phi_t}\right) + \frac{\psi}{\phi_t} - 1\right) + \left(\exp\left(\frac{\psi}{\phi_t}\right) - \frac{\psi}{\phi_t} - 1\right)\right] , \tag{2.30}$$

$$L_D = \sqrt{\frac{\epsilon_s \phi_t}{qN_D}} . \tag{2.31}$$

From Eqn. 2.29, the surface field is given by $\mathcal{E}_s = \pm\frac{\sqrt{2}\phi_t}{L_D}\mathcal{F}(\psi_s)$ and the surface charge per unit area can be obtained by Gauss law

$$Q_s = -\epsilon_s \mathcal{E}_s = \mp\frac{\sqrt{2}\epsilon_s \phi_t}{L_D}\mathcal{F}(\psi_s) . \tag{2.32}$$

This equation is valid for all ψ_s, i.e. for accumulation, depletion and inversion. The capacitance of the depletion layer can be derived using Eqn. 2.32:

$$C_D = \frac{\partial Q_s}{\partial \psi_s} = -\frac{\epsilon_s}{\sqrt{2}L_D}\frac{\frac{n_i^2}{N_D^2}\left(1 - e^{-\frac{\psi_s}{\phi_t}}\right) + e^{\frac{\psi_s}{\phi_t}} - 1}{\mathcal{F}(\psi_s)} . \tag{2.33}$$

By means of series expansion of the exponential terms of Eqn. 2.33, the capacitance of the depletion layer at flat-band condition $\psi_s = 0$ can be obtained as

$$C_D(\psi_s = 0) = \frac{\epsilon_s}{L_D} . \tag{2.34}$$

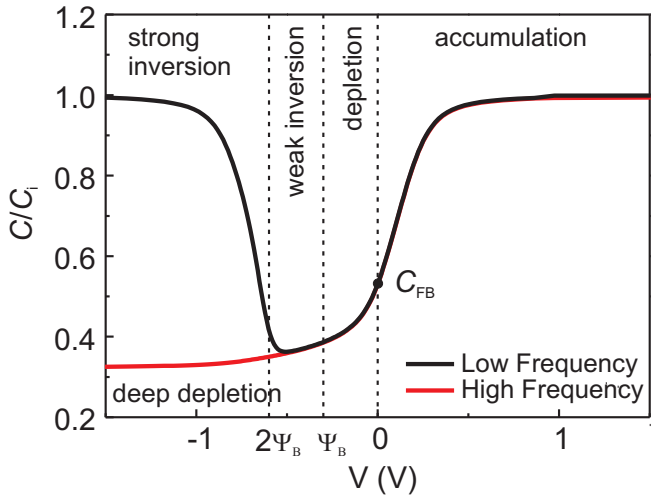


Figure 2.4: Ideal CV characteristic of a ZnO MIS diode for high and low measurement frequencies.

An applied external voltage V will partially drop across the insulator and the semiconductor:

$$V = V_\mathrm{i} + \psi_\mathrm{s} \ , \tag{2.35}$$

where

$$V_\mathrm{i} = \frac{|Q_\mathrm{s}|}{C_\mathrm{i}} = \frac{|Q_\mathrm{s}|d}{\epsilon_\mathrm{i}} \tag{2.36}$$

is the voltage drop across the insulator and C_i is the insulator capacitance per unit area with $\epsilon_\mathrm{i} = \kappa\epsilon_0$ being the insulator permittivity and κ being the dielectric constant of the insulator.

A change of the applied voltage V will also effect V_i and ψ_s to equalize the system. Charge neutrality has to be considered:

$$Q_\mathrm{m} = -(Q_\mathrm{p} + Q_\mathrm{D}) \ , \tag{2.37}$$

where Q_m is the charge at the metal gate, Q_p is the charge in the inversion layer and $Q_\mathrm{D} = qwN_\mathrm{D}$ is the depletion layer charge.

The total capacitance of the MIS diode can now be determined considering it as a capacitor with a dielectric in series to the depletion layer and combining Eqns. 2.33, 2.35 and 2.36:

$$C = \frac{1}{\frac{1}{C_\mathrm{i}} + \frac{1}{C_\mathrm{D}}} \ . \tag{2.38}$$

The ideal CV characteristic for a ZnO MIS diode obtained from Eqn. 2.38 is shown in Fig. 2.4.

In accumulation ($V > 0$), the total capacitance is close to the insulator capacitance due to screening of the charges in the semiconductor by accumulated electrons at the insulator-semiconductor interface. The capacitance at flat-band condition is obtained from Eqns. 2.34 and 2.38:

$$C_{\mathrm{FB}} = \left(\frac{d}{\epsilon_{\mathrm{i}}} + \frac{L_{\mathrm{D}}}{\epsilon_{\mathrm{s}}} \right)^{-1} . \tag{2.39}$$

For voltages smaller than the flat-band voltage V_{FB} , the depletion region is formed and, according to Eqn. 2.38, the total capacitance decreases. The depletion region can be analyzed analogous to the Schottky diode (Sec. 2.1.2); the net doping concentration can be obtained from Eqn. 2.8.

The ideal CV characteristic (Fig. 2.4) passes a minimum and then increases in the inversion regime. However, this depends on the measurement frequency. At low frequency, the generation rate of minority carriers can follow the voltage signal. As a large voltage is applied, the strong inversion regime occurs and from Eqn. 2.21 the surface potential is then [Tsi03]:

$$\psi_{\mathrm{s}}^{\mathrm{inv}} \cong 2\psi_{\mathrm{B}} = 2\phi_{\mathrm{t}} \ln \frac{N_{\mathrm{D}}}{n_{\mathrm{i}}} , \tag{2.40}$$

where the hole density becomes equal to the majority carrier concentration. The inversion layer screens the semiconductor from the electric field and the total capacitance C equals the insulator capacitance C_{i} again.

For high frequency, the MIS capacitance does not increase again. This case is called deep depletion (cf. Fig. 2.4). The variation in the voltage signal is too fast to modulate the minority carrier density.

In large band gap semiconductors such as GaN [Has00] and ZnO, the inversion case of the MIS CV measurement can not be easily observed. It can be shown from [Zeg04], that the minimum rate of time required for inversion can be approximated by the ratio of the total charge of the inversion layer $|Q_{\mathrm{p}}|$ and the generation rate G of minority carriers. Simplifying the case to only consider generation in the neutral region, the required time and voltage change per time is given by:

$$t = \frac{Q_{\mathrm{p}}}{qGL_{\mathrm{n}}} \frac{dV}{dt} < \frac{qGL_{\mathrm{n}}}{C_{\mathrm{i}}} = \frac{qn_{\mathrm{i}}}{2C_{\mathrm{i}}} \sqrt{\frac{\mu_{\mathrm{n}}\phi_{\mathrm{t}}}{\tau_{\mathrm{n}}}}, \tag{2.41}$$

where τ_{n} is the carrier lifetime, L_{n} is the diffusion length and μ_{n} is the electron mobility. For ZnO, it can be estimated with typical values of $\tau_{\mathrm{n}} \sim 1\ \mu$s, $dV = 0.1$ V, $C_{\mathrm{i}} \sim 1 \times 10^{-7}$ F/cm^2, $\mu_{\mathrm{n}} \sim 50$ cm^2/Vs and $n_{\mathrm{i}} \sim 10^0$ cm^{-3} [Man06, Pea04]. The approximate minimum measurement time for one data point in CV measurements to see inversion in ZnO would be

$$dt > 10^8 \text{ s} . \tag{2.42}$$

Thus, it is hard to observe inversion in ZnO MIS diodes in thermal equilibrium.

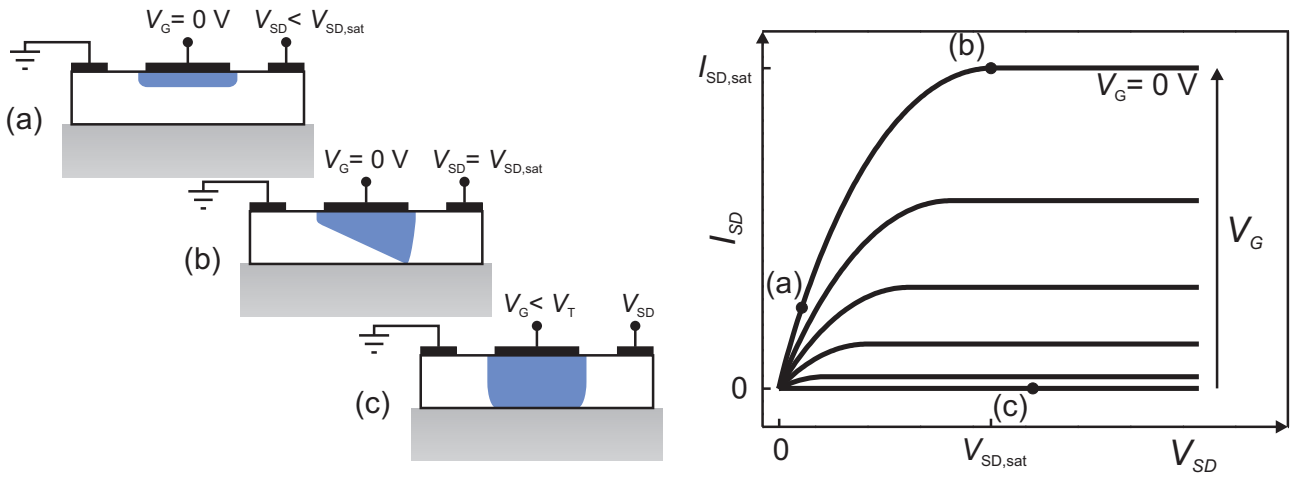


Figure 2.5: General principle and schematic output characteristic of a MESFET.

2.3 Operation principles of unipolar field-effect transistors

2.3.1 Metal-semiconductor field-effect transistors

Operation principle

On behalf of using ZnO as channel material, the general principle (Fig. 2.5) of a *n*-type, normally-on MESFET shall be considered in this section. For a gate voltage $V_G = 0$ V and a source-drain voltage of $V_{SD} = 0$ V, the transistor is in thermodynamic equilibrium; no currents occur. By increasing $V_{SD} > 0$, a source-drain current I_{SD} will flow due to the electric field between source and drain. Initially, for low V_{SD}, the channel resistance is constant and I_{SD} depends linearly on V_{SD} according to Ohm's law (cf. Fig. 2.5a). With increasing V_{SD}, the voltage drop across the channel and the corresponding potential difference leads to an expansion of the depletion layer at the drain side of the channel, which is larger at the drain side of the channel. At a certain voltage, called saturation voltage $V_{SD,sat}$, the depletion layer width equals the channel thickness, i.e. the channel is pinched off (Fig. 2.5b). A further increase of V_{SD} to $V_{SD,sat} + \Delta V$ shifts the pinch-off point towards the source contact and ΔV drops across the laterally expanded depletion layer. The voltage drop in the remaining open channel (from source to the pinch-off point) remains therefore constant at $V_{SD,sat}$. Thus, according to Kirchoff's law, the diffusive source-drain current saturates ($I_{SD}(V_{SD} > V_{SD,sat}) = I_{SD,sat}$). An excessive increase of V_{SD} results in the breakdown of the channel. Impact ionization leads to increased generation of electron-hole pairs and I_{SD} will uncontrollably increase.

The cross-section of the conducting channel can also be controlled by varying the gate voltage V_G. The width of the depletion region under the Schottky gate-contact can be expanded according to Eqn. 2.7, such that the complete channel is depleted and $I_{SD} = 0$ for all applied V_{SD} (Fig. 2.5c). The gate voltage needed to completely close the channel is called turn-on voltage V_T. With increasing negative V_G and constant V_{SD}, the ohmic resistance in the linear regime of the output characteristic increases due to the decreasing cross-section of the conducting channel. The pinch-off at the drain contact is then already reached for smaller V_{SD}, i.e. $V_{SD,sat} \rightarrow 0$ for $V_G \rightarrow V_T$. This implies, that a decreasing

part of the constant V_{SD} drops over the non-depleted part of the channel and I_{SD} is decreasing until, finally, $V_{SD,sat} = 0$ and $I_{SD} = 0$ in the ideal case.

Current-voltage characteristic

For the derivation of the current-voltage characteristic of a MESFET, the following assumptions are made:

1. The lateral direction, parallel to the substrate is referred to a x-direction.
2. The channel is homogeneously doped with a doping concentration N_D.
3. The size of the depletion layer is slowly changing in x-direction ($\mathcal{E}_x \ll \mathcal{E}_y$, "gradual channel approximation").
4. The length of the gate is larger than the channel thickness ($L \gg d$, "long-channel approximation").
5. The mobility of the electrons is constant ($v = \mu\mathcal{E}_x$).
6. The current over the gate is negligible.

The drift current density is given by the mobile charges in the channel ($n = N_D$) and their velocity:

$$j(x) = Qv(x) = -qN_D\mu\mathcal{E}_x = qN_D\mu\frac{\partial V}{\partial x} \; . \tag{2.43}$$

Therefore, the source-drain current in the neutral part of the channel with cross-section $A = W(d - w(x))$, W being the channel width and $w(x) = \sqrt{\frac{2\epsilon_r\epsilon_0}{eN_D}(V_{bi} + V_G + V(x))}$ being the depletion layer depth according to Eqn. 2.7, is given by

$$I_{SD}(x) = j(x)A = qN_D\mu\frac{dV}{dx}(d - w(x))W \; . \tag{2.44}$$

I_{SD} is constant along the channel due to Kirchhoff's second law; i.e. with $\int_0^L I_{SD}(x)dx = LI_{SD}$:

$$I_{SD} = \frac{qN_D\mu W}{L}\int_0^L \frac{dV}{dx}(d - w(x))dx \tag{2.45}$$

$$= \frac{qN_D\mu W}{L}\int_0^{V_{SD}} \left(d - \sqrt{\frac{2\epsilon_r\epsilon_0}{qN_D}(V_{bi} + V_G + V)}\right)dV. \tag{2.46}$$

The solution of this integral can be written as [Sze81, Zeg04]:

$$I_{SD} = g_{max}\left(V_{SD} - \frac{2}{3\sqrt{V_P}}\left[(V_{bi} + V_{SD} + V_G)^{3/2} - (V_{bi} + V_G)^{3/2}\right]\right) \; , \tag{2.47}$$

where

$$g_{\max} = \frac{q\mu N_{\mathrm{D}} dW}{L} \tag{2.48}$$

is the maximum transconductance of the channel obtained for $w = 0$ and

$$V_{\mathrm{P}} = \frac{qN_{\mathrm{D}} d^2}{2\epsilon_{\mathrm{r}}\epsilon_0} \tag{2.49}$$

being the pinch-off voltage obtained for $w = d$.
Eqn. 2.47 is valid as long as the width of the undepleted channel $d - w(x)$ is positive, i.e. for

$$V_{\mathrm{SD}} \leq V_{\mathrm{G}} - V_{\mathrm{T}} \,, \tag{2.50}$$

where $V_{\mathrm{T}} = V_{\mathrm{bi}} - V_{\mathrm{P}}$ is the threshold voltage of the MESFET.
For small V_{SD}, Eqn. 2.47 can be linearized to

$$I_{\mathrm{SD}} = g_{\max}\left(1 - \sqrt{\frac{V_{\mathrm{bi}} + V_{\mathrm{G}}}{V_{\mathrm{P}}}}\right) V_{\mathrm{SD}} \propto V_{\mathrm{SD}} \,. \tag{2.51}$$

With further increasing V_{SD}, I_{SD} saturates. Inserting the saturation voltage $V_{\mathrm{SD,sat}} = V_{\mathrm{G}} - V_{\mathrm{T}}$ into Eqn. 2.47 leads to the saturation current

$$I_{\mathrm{SD,sat}} = g_{\max}\left(V_{\mathrm{G}} - V_{\mathrm{T}} - \frac{2}{3}\left(V_{\mathrm{P}} - \frac{(V_{\mathrm{bi}} - V_{\mathrm{G}})^{3/2}}{\sqrt{V_{\mathrm{P}}}}\right)\right) \,. \tag{2.52}$$

The MESFET channel mobility can now be determined either from the output characteristic $I_{\mathrm{SD}}(V_{\mathrm{SD}})$ for $V_{\mathrm{SD}} \to 0$ using the drain transconductance g_{D0} or from the transfer characteristic in the saturation regime $I_{\mathrm{SD,sat}}(V_{\mathrm{G}})$ using the saturation forward transconductance $g_{\mathrm{m,sat}}$. The relation between both values is

$$g_{\mathrm{D0}} = \left.\frac{\partial I_{\mathrm{SD}}}{\partial V_{\mathrm{SD}}}\right|_{V_{\mathrm{SD}}\to 0} = g_{\max}\left[1 - \left(\frac{V_{\mathrm{bi}} + V_{\mathrm{G}}}{V_{\mathrm{P}}}\right)^{1/2}\right] = \frac{\partial I_{\mathrm{SD,sat}}}{\partial V_{\mathrm{G}}} = g_{\mathrm{m,sat}} \,. \tag{2.53}$$

From Eqn. 2.53, $g_{\max}$ can be extracted and inserted in Eqn. 2.48. The channel mobility is then given by

$$\mu_{\mathrm{ch}} = \frac{g_{\max}}{qN_{\mathrm{D}} d(W/L)} \,. \tag{2.54}$$

2.3.2 Metal-insulator-semiconductor field-effect transistors

As described in Sec. 2.2.2, inversion cannot be achieved for ZnO MISFET in thermodynamic equilibrium. For this reason, a MISFET model is considered, where no inversion charge occurs. Instead in an electrostatic approach, the induced charge Q_{ind} within the channel of the transistor is given by the insulator capacitance C_{i} and the difference between applied gate voltage and turn-on voltage $V_{\mathrm{G}} - V_{\mathrm{T}}$:

$$Q_{\mathrm{ind}} = -C_{\mathrm{i}}(V_{\mathrm{G}} - V_{\mathrm{T}}) \,, \tag{2.55}$$

assuming that the charge density is constant along the channel. The source-drain current according to Eqn. 2.43 is then given by

$$I_{\mathrm{SD}} = -Q_{\mathrm{ind}} v W = -Q_{\mathrm{ind}} \mu \frac{W}{L} \cdot V_{\mathrm{SD}} \,, \tag{2.56}$$

where $v = \mu\mathcal{E} = \mu\frac{V_{\mathrm{SD}}}{L}$ is the charge carrier's velocity. Inserting Eqn. 2.55 into Eqn. 2.56 leads to

$$I_{\mathrm{SD}} = \mu C_{\mathrm{i}} \frac{W}{L}(V_{\mathrm{G}} - V_{\mathrm{T}})V_{\mathrm{SD}} \,. \tag{2.57}$$

This is the linear model of the MISFET [Zeg04], which is valid for small V_{SD}, where the transistor acts like a linear resistor whose resistance is modulated by V_{G}.

Taking into account that the electric field varies along the channel from source to drain, as it does for the MESFET, a small section dx and a local channel voltage V_{C} is considered. The linear model (Eqn. 2.57) still applies for this section, yielding:

$$I_{\mathrm{SD}} = \mu C_{\mathrm{i}} \frac{W}{dx}(V_{\mathrm{G}} - V_{\mathrm{C}} - V_{\mathrm{T}})dV_{\mathrm{C}} \,. \tag{2.58}$$

Both sides can be integrated from source to drain, again with I_{SD} being constant due to Kirchhoff's second law.

$$\int_0^L I_{\mathrm{SD}} dx = \mu C_{\mathrm{i}} W \int_0^{V_{\mathrm{SD}}} (V_{\mathrm{G}} - V_{\mathrm{C}} - V_{\mathrm{T}})dV_{\mathrm{C}} \tag{2.59}$$

The integration results in:

$$I_{\mathrm{SD}} = \mu C_{\mathrm{i}} \frac{W}{L}\left[(V_{\mathrm{G}} - V_{\mathrm{T}})V_{\mathrm{SD}} - \frac{V_{\mathrm{SD}}^2}{2}\right] \,. \tag{2.60}$$

I_{SD} first increases linearly with V_{SD} before it reaches a maximum value and saturates due to the pinch-off of the channel at the drain side. For the saturation voltage $V_{\mathrm{SD,sat}} = V_{\mathrm{G}} - V_{\mathrm{T}}$, the saturation current is given by

$$I_{\mathrm{SD,sat}} = \mu C_{\mathrm{i}} \frac{W}{L} \frac{(V_{\mathrm{G}} - V_{\mathrm{T}})^2}{2} \,. \tag{2.61}$$

Eqn. 2.61 is usually applied for the mobility extraction of MISFET, plotting $\sqrt{I_{\mathrm{SD,sat}}}$ versus V_{G} and using the slope of the resulting linear function. However, since ZnO-based MISFET do not always show the ideal linear behavior of this plot, the obtained mobility is defective [Hof04]. In this case, it is better to use the saturation transconductance

$$g_{\mathrm{m,sat}} = \frac{\partial I_{\mathrm{SD,sat}}}{\partial V_{\mathrm{G}}} = \mu C_{\mathrm{i}} \frac{W}{L}(V_{\mathrm{G}} - V_{\mathrm{T}}) \; . \tag{2.62}$$

The channel mobility is then given by

$$\mu_{\mathrm{ch}} = \frac{g_{\mathrm{m,sat}}}{\frac{W}{L} C_{\mathrm{i}}(V_{\mathrm{G}} - V_{\mathrm{T}})} \; . \tag{2.63}$$

2.4 Integrated Logic Circuits

Integrated circuits are the basis for today's complex electronics, e.g. computational devices (microchips), sensors, amplifiers etc. Integration of different electronic devices on a small area leads to manifold functionality and reduces fabrication costs. The first integrated circuit was developed by J. Kilby in 1958 [Kil76]. It was a hybrid flip-flop[1] consisting of two bipolar transistors on germanium substrate that were interconnected with gold wires. However, the first monolithic IC, i.e. fabricated on one single-crystalline substrate including transistors and interconnects, was patented in 1959 by R. Noyce [Noy61].

This thesis deals with two physical realizations of elements of the logic or Boolean algebra [Boo54]: the inverter and the NOR-gate. The truth tables and graphical symbols of these elements are shown in Fig. 2.6. With the help of Boole's laws, the logic elements "true" (1) and "false" (0) are linked together to more complex information. In circuits, this is realized by a high voltage level (true, 1) and a low level (false, 0). The basic logic element is the inverter (or NOT-gate). It is a device with one input and one output. the output is logic 1 only in the case, when the input is a logic 0 and vice versa. The NOR-gate represents the composed function "not-or". It is a device with two inputs and one output. The output gives the logic 1 only in the case, when none of the inputs are logic 1. It can be shown [Mor47], that it is possible to create a complete logic, e.g. including all possible statements, only by using NOR- and NOT-gates.

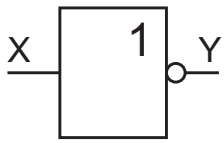
2.4.1 Physical realization of the NOT function

In the most common realization (the CMOS[2]-technology), an inverter consists of one *n*-conducting MOSFET and one *p*-conducting MOSFET connected in series (Fig. 2.7). The transistors serve as complementary voltage-driven switches. The circuit is supplied with the voltage V_{DD}. If the input voltage V_{in} is low (logic 0), only the *p*-channel transistor is conducting; the output voltage equals the supply voltage $V_{\mathrm{out}} = V_{\mathrm{DD}}$, i.e. the output level is high (logic 1). For $V_{\mathrm{in}} > 0$ (typically > 1 V, logic

[1] A flip-flop is a circuit that can switch and store two stable states.
[2] Complementary Metal-Oxide-Semiconductor

(a)

X	$Y=\overline{X}$
0	1
1	0



(b)

A	B	$Y=\overline{A \vee B}$
0	0	1
0	1	0
1	0	0
1	1	0

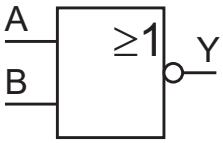


Figure 2.6: Truth table and graphical symbol of a) a NOT-gate or inverter and b) a NOR-gate.

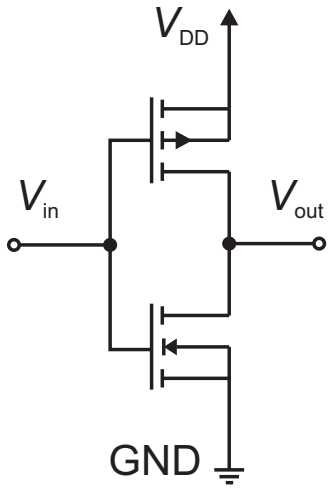


Figure 2.7: Circuit of a CMOS inverter.

1), the *n*-channel transistor is conducting and V_{DD} is grounded; i.e. $V_{out} = 0$ V (logic 0). Since *n*- and *p*-type transistors are easily fabricated in silicon technology, this type of inverter is the basic for today's integrated circuitry.

A schematic voltage transfer curve (VTC) is depicted in Fig. 2.8. It serves as quantification of the inverter function and its figures of merit shall be defined in the following paragraphs.

In the ideal case, the resistances of the inverter's transistors are infinite if they are in the off-state, and equal to zero in the on-state. This would lead to the ideal VTC, where the output high level equals the supply voltage ($V_{OH} = V_{DD}$) and the output low level is exactly zero ($V_{OL} = 0$ V). The ideal inverter would switch at $V_{DD}/2$. The slope of the VTC would be infinite and the state of the inverter is uncertain only at this single point.

The real inverter is determined by the finite resistances of its transistors. So, there must be a transition range where the inverter switches from high to low level. The slope of this range equals to the gain of the inverter obtained if it was used as a voltage amplifier:

$$g = \left| \frac{\partial V_{out}}{\partial V_{in}} \right| . \tag{2.64}$$

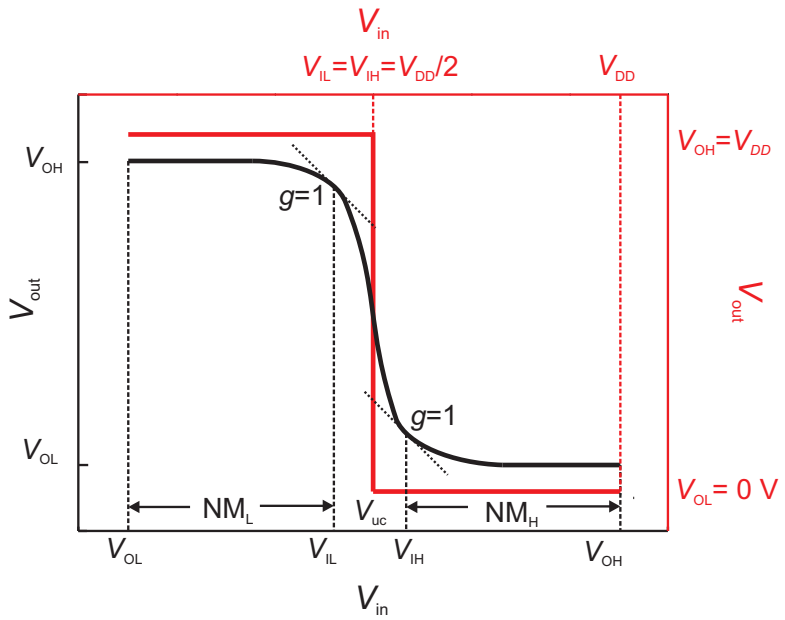


Figure 2.8: Voltage-transfer curve of an ideal and a real inverter.

The maximum of g is denoted as peak gain magnitude (*pgm*). The input voltage, where *pgm* is achieved, is called reversal voltage V_{rev}. The borders of the transition range are marked with the input low and high voltages V_{IL} and V_{IH}, where $g = 1$. V_{IL} is the maximal input voltage for which the output level is clearly high. The other way around, V_{IH} is the minimal input voltage for which the output level is clearly low. Their difference is called uncertainty voltage range:

$$V_{\text{uc}} = V_{\text{IH}} - V_{\text{IL}} \ . \tag{2.65}$$

Left and right from the uncertainty voltage range are the regions for which the inverter output level is unambiguously defined. These regions are denoted as noise margins [Sed04]:

$$NM_{\text{L}} = V_{\text{IL}} - V_{\text{OL}}, \tag{2.66}$$
$$NM_{\text{H}} = V_{\text{OH}} - V_{\text{IH}}. \tag{2.67}$$

For the ideal inverter, the noise margins would be equal and maximal $NM_{\text{L}} = NM_{\text{H}} = V_{\text{DD}}/2$. However, in the case of a non-ideal inverter, where $g = 1$ at two points of the input voltage, the noise margins would be ambiguous. Therefore J. Hauser suggested to maximize the product $NM_{\text{L}} \times NM_{\text{H}}$ as figure of merit [Hau93].

2.4.2 MESFET-based inverter circuits

In the framework of this thesis, ZnO-MESFET-based inverter circuits were designed and fabricated. MESFET were used for the sake of their advantages, e.g. higher mobility and lower operation voltages, compared to MISFET. However, there are two constraints about ZnO-based MESFET: a) The

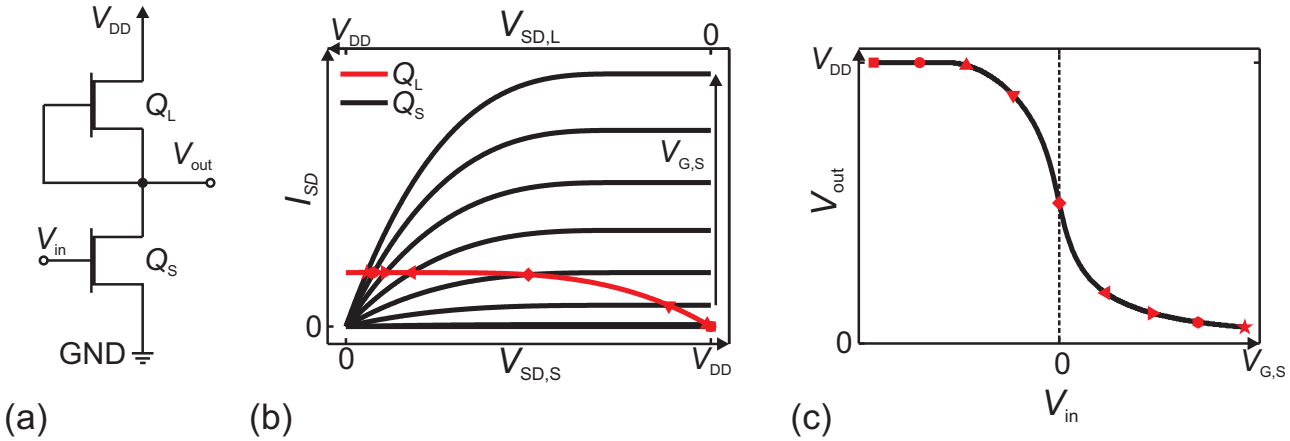


Figure 2.9: a) Circuit of a simple MESFET inverter, b) Output characteristics of the transistors, c) resulting voltage-transfer characteristic.

complementary design is not possible due to the absence of *p*-type transistors. b) The forward gate-voltage of a MESFET is restricted due to excessive gate leakage currents; an accumulation mode is not possible. Similar problems are known from the GaAs-MESFET technology. It has a five to ten times higher electron mobility compared to Si [Sed04] enabling the fabrication of transistors and circuits that can easily work in the GHz-range. But the hole mobility of GaAs is much lower, making *p*-type transistors and complementary circuits unattractive. The circuits used in this thesis were adopted from GaAs-MESFET logic described in [Sed04].

Simple Inverter

Figure 2.9a depicts the circuit of a simple MESFET inverter. Two normally-on MESFET are connected in series. The upper FET is denoted as load transistor Q_L, whereas the lower FET is the switching transistor Q_S. The source- and gate-contact of Q_L is shortcircuited. Thus, its gate voltage is constant $V_{G,L} = 0\,V$ and the transistor is in the linear or saturation regime, respectively, depending on the operating voltage V_{DD} (which is related to the source-drain voltage $V_{SD,L}$ of Q_L). The state of Q_S can be controlled via the input voltage V_{in} (which is the gate voltage $V_{G,S}$ of Q_S).

The formation of the inverter's VTC is related to the transistor's output characteristics. Figure 2.9b shows the output characteristics of Q_S in the voltage range between 0 V and V_{DD} with $V_{G,S}$ as parameter. In the same graph, the single output curve of Q_L, which is set to $V_{G,L} = 0\,V$, is drawn with reversed voltage axis. According to Kirchhoff's second law, the source-drain voltages are related to the operation voltage by

$$V_{SD,S} + V_{SD,L} = V_{DD}\,. \tag{2.68}$$

The intersection points of both characteristics represent the working points of the switching transistor, where both transistors carry the same current. With $V_{SD,S} = V_{out}$, these points reproduce the inverter's VTC (Fig. 2.9c). It can be seen, that it will be difficult to reach $V_{out} = 0\,V$, because then, the linear

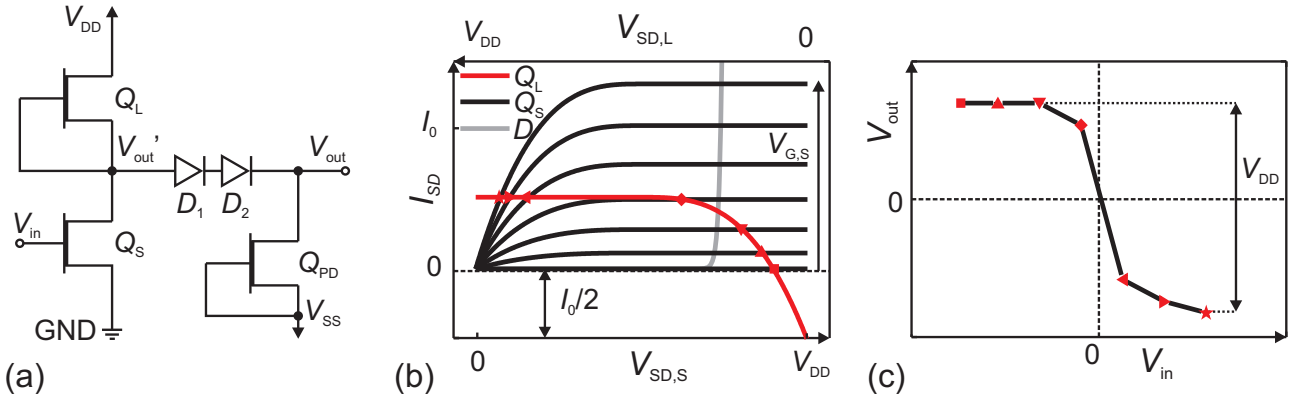


Figure 2.10: a) Circuit and b) Characteristics of the transistors/diodes and c) the FET-logic inverter.

regime of the output characteristic of Q_S, has to be infinitely steep, i.e. the channel resistance has to be zero.

Since both transistor's resistances are equal at $V_{G,S} = V_{G,L} = 0\,V$, the switching point of the inverter is at $V_{in} = 0\,V$. This is, however, the central problem of the simple inverter whose output voltage V_{out} is always positive. For the high output of the inverter, V_{in} has to be $V_{T,S} < V_{in} < 0$, due to the higher resistance of Q_S in this voltage range. In order to turn Q_S off, the input voltage has to be lower than its turn-on voltage; i.e. $V_{in} = V_{G,S} \leq V_{T,S} < 0$. If two or more inverters are connected in series, e.g. for a ring oscillator, the output of the subsequent inverter can never securely be logic high level, due to the first inverter's output is always positive. To circumvent this incompatibility, an additional level-shifting part has to be implemented into the circuit, as described in the following section.

FET-logic Inverter

For the realization of inverter with level-shifter, the FET-logic (FL) is adopted from GaAs-MESFET technology. It was first developed by R. L. van Tuyl and C. A. Liechti in 1974 [Tuy74]. This logic family comprises additional Schottky diodes and transistors to adjust the voltage levels by means of the voltage drop over the diodes.

Figure 2.10a depicts the circuit of a FL-inverter consisting of the simple inverter part and the level shifter. The level shifter (LS) comprises two Schottky diodes D_1 and D_2 and an additional pull-down transistor Q_{PD} connected in series at the output of the simple inverter. The voltage drop across the two diodes lowers the former output level V'_{out} to $V_{out} = V'_{out} - 2V_x$, where V_x is the threshold voltage of the diode. Q_{PD} serves as constant-current supply for the diodes. To ensure that Q_{PD} is always in saturation, a negative V_{SS} with $V_{SS} \geq V_{OL} + |V_T|$ is applied at its source contact. The pull-down transistor's gate width is chosen to be half of the gate widths of Q_L and Q_S. Furthermore, Q_{PD} provides the current to discharge a parasitic load capacity, when the inverter output level is low.

The VTC of the FL-inverter can be determined graphically analog the simple inverter (Fig. 2.9b and c). The corresponding graphs are given in Fig. 2.10b and c. For $V_{in} = V_{G,S} < V_{T,S}$, Q_S is in the off-state; for $V_{G,S} = 0\,V$, the saturation current I_0 flows. The current through Q_L is composed of the currents through Q_S and Q_{PD}, i.e. $I_L = I_S + I_{PD}$. Since the gate width of Q_{PD} is half of the other

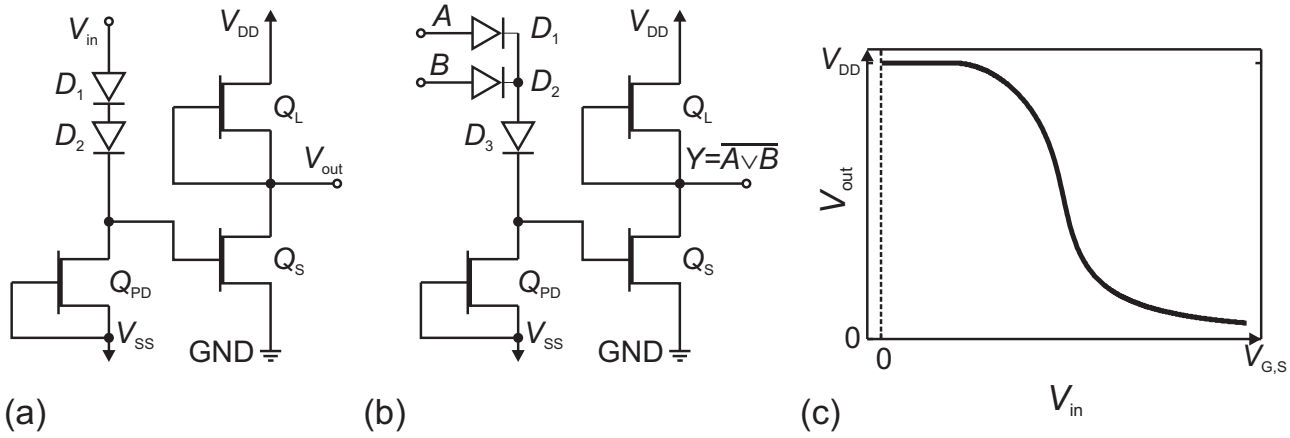


Figure 2.11: a) Circuit of a Schottky-diode FET-logic (SDFL) inverter and b) a SDFL NOR-gate. c) Characteristic of a SDFL-inverter.

transistors' gate widths, its current is only half of the other currents (cf. Eqns. 2.48 and 2.52), i.e. the load transistor output characteristic is shifted to $I_S = I_L - I_{PD} = I_L - I_0/2$. Furthermore, V'_{out} cannot exceed $V_{out} = 3V_x$, where $V_{out} = V_x$ is the threshold voltage of the subsequent gate Schottky diode. Graphically, only the intersection points left of the three-diode characteristic are considered. The VTC of the FL-inverter is shifted towards negative output voltages (Fig. 2.10c). That means, the output low level is lower than the turn-on voltage of the subsequent inverter's gate, i.e. $V_{OL} < V_{T,S}$ and secure inverter states are achieved.

An advantage of the FL-inverter is the usage of equal normally-on MESFET for the circuit. On the other hand, two voltage sources are needed and in contrast to CMOS, a current flows permanently.

When the level shifter part is connected at the input of the simple inverter, the circuit (Fig. 2.11a) is called Schottky-diode FET-logic (SDFL) inverter. It was developed in the late 1970's by B. M. Welch and R. C. Eden [Wel77, Ede77, Ede78a, Ede78b, Ede81]. This circuit can easily be expanded by one additional Schottky diode D_3 implementing a NOR-gate (Fig. 2.11b). Due to the level-shifter, the gate voltage of Q_S is shifted by the voltage drop across the two diodes, i.e. $V_{G,S} = V_{in} - 2V_x$. Consequently, the VTC of the SDFL-inverter is shifted towards positive input voltages. Due to the shift, the ouput low level of the inverter is always lower than the gate voltage of a subsequent inverter and secure inverter states are achieved as for the FL-inverter.

3 Device fabrication and characterization

3.1 Pulsed-laser deposition

The conducting, semiconducting and insulating oxide thin films used in this thesis as transparent contact, channel layer and gate oxide, respectively, were fabricated by Holger Hochmuth at Universität Leipzig using pulsed-laser deposition (PLD). The growth process is devided into three parts [Lor08]. First, high-power laser pulses with an energy density in the range of 10^8 W/cm^2 are directed on a target. The PLD targets were mixed, pressed and sintered by Gabriele Ramm (Universität Leipzig) from ZnO, MgO, Al_2O_3, HfO_2 and ZrO_2 powders. The laser energy is absorbed in the target material which melts, evaporizes and ionizes; a plasma plume is developed. Atoms, ions and particles are transported in the plasma plume to the surface of the heated substrate, condensate and form an oxide thin film. The parameters of PLD growth, used in this thesis are given in Tab. 3.1.

One advantage of the PLD is the perpetuation of the stoichiometry of the target in the resulting film. The single components are not mixed during growth, but the chemical composition is pre-defined in the mixing of the target. Thus, it is easy to grow multiple-component mixed crytals. Another advantage is the control of the film thickness by the number of pulses. For the growth of one monolayer, 5 to 10 laser pulses are needed. The growth rate on the used sapphire and glass substrates lies in the range of several ten nanometers per minute.

Disadvantages of the used PLD-system are e.g. the limitation of the substrate size by the size of the plasma plume. The maximum substrate diameter that have been used during this thesis is two inch. Furthermore, also larger particles ($\sim 1\,\mu$m) can be separated from the target and deposited as droplets within the oxide layer on the substrate. The fundamental processes of PLD are not yet fully understood. Thus, the introduction of new materials is complicated and needs empiric optimization.

Besides the parameters listed in Tab. 3.1, the properties of the grown thin films are also influenced by effects that tend to reduce their reproducability. These are, for example, deposition of material

Table 3.1: Parameters of the used PLD system.

Parameter	Value
laser	KrF excimer laser (λ = 248 nm)
frequency	1-50 Hz
pulse energy	600 mJ
target-substrate distance	10 cm
oxygen partial pressure	3×10^{-4} – 1 mbar
substrate temperature	25 - 700°C
heater power	0 – 500 W

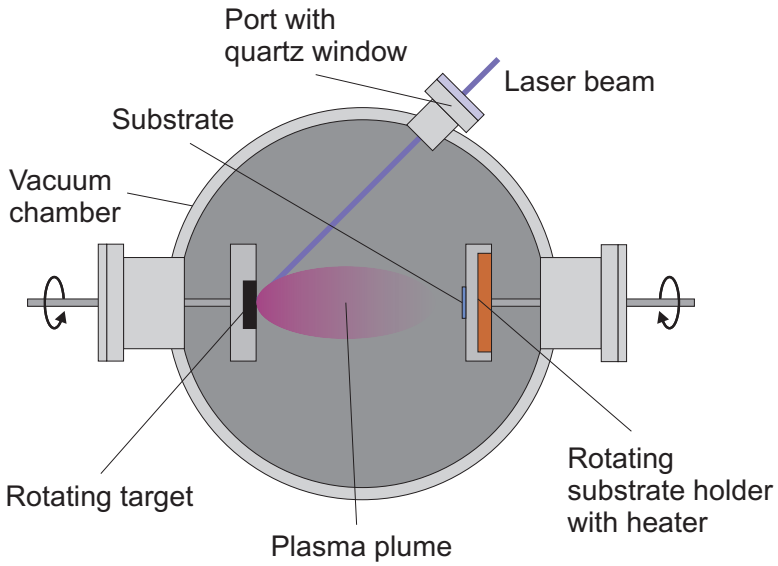


Figure 3.1: Scheme of a pulsed-laser deposition system.

on the chamber window which leads to a reduction of the laser energy on the target, or the grade of target ablation – the deeper the ablation crater on the target, the more oscillation of the plasma plume around the target normal occurs. Further, evaporation of substrate-heater material contaminates the growing layer. Memory effects of previously grown materials occur and the history of the target plays an important role. Material can be deposited on the surface of an unused target (which stays in the chamber), leading to contamination of the next film grown with this target. For this reason, it is important to pre-sputter the targets with some laser pulses. During this work, a ZnO and MgZnO target were exclusively used for the growth of the channel layer of the FET and inverters to ensure maximum reproducibility.

3.2 Direct-current sputtering

The ohmic and rectifying contacts, that have been used during this thesis, were fabricated by means of direct-current (DC) sputtering mostly operated by Hannes Münch (Universität Leipzig). The setup and modes of operation are depicted in Fig. 3.2. The vacuum chamber is flooded under low pressure with the inert gas argon. A high voltage is applied between the cathode, where the metallic target is mounted and anode, where the substrate lies. By means of impact ionization, a plasma is formed. Due to the electric field, the positively charged Ar ions are accelerated towards the target, where they separate neutral metal atoms, which are moving to the substrate and form a thin film.

The standard sputter parameters for the Schottky contacts were found by Alexander Lajn (Universität Leipzig) and are given in Tab. 3.2.

The ohmic contacts and conducting capping layers on the Schottky-contacts were non-reactively sputtered, i.e. with pure Ar in the chamber. The functional Schottky-contact layers were reactively sputtered under an Ar/O_2-flux ratio of 50 sccm/50 sccm. The oxygen partially oxidizes the sputter-target

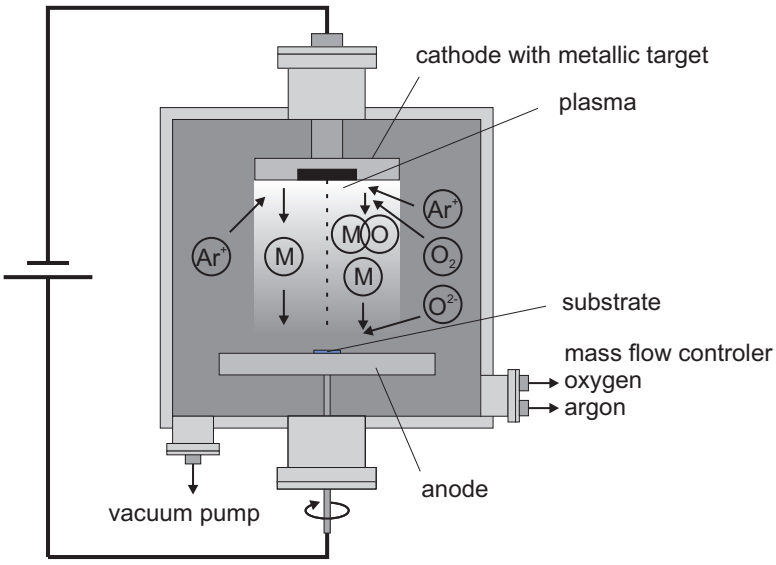


Figure 3.2: Schematic setup of the sputter chamber and principle of non-reactive (left of dashed line) and reactive (right) sputtering. M: metal atoms, MO: metal-oxide compound.

Table 3.2: Standard sputter parameters of ohmic as well as opaque and transparent rectifying contacts.

	ohmic	Schottky (opaque)	Schottky (transparent)
power	30 W	30 W	5 W
target-substrate distance	4 cm	4 cm	4 cm
target	Au	Ag, Pt, Pd, Au	Ag, Pt
target (capping)	-	Au	Au, Pt
sputter time	25 s	25 s	30 s
sputter time (capping)	-	15 s	10 s
gas pressure	0.024 mbar	0.028 mbar	0.028 mbar
Ar-flux	100 sccm	50 sccm	50 sccm
O_2-flux	0	50 sccm	50 sccm

material such that metal as well as metaloxide particles are deposited on the substrate.

There are two reasons why the reactive sputtering process leads to an improvement of the Schottky contacts. On the one hand, the negatively charged oxygen ions bombard the substrate's surface during the initial phase of the deposition process. Thus, an in-situ plasma surface cleaning is achieved, which probably leads to the removal of a hydroxide-induced, highly conductive surface layer that reduces the Schottky barrier height [Cop03]. On the other hand, the contact material (except Au) is oxidized, which has been investigated by means of X-ray photoelectron spectroscopy [Laj09]. This coincides with an increase of the work function and with that leads to higher Schottky barrier heights on single crystalline ZnO substrates [All07, All09] as well as on heteroepitaxially grown ZnO thin films on sapphire [Laj09].

Due to the oxidation of the Schottky-metals, their conductivity is significantly lower than that of pure metals. Therefore, it is necessary to deposit a metallic conducting capping layer on top of the Schottky

contact in order to form an equipotential surface.

3.3 Photolithography

The PLD-grown samples consist of a thin (~ 30 nm) ZnO-based channel layer on top of an insulating substrate. The processing of devices is carried out by means of photolithography, wet-chemical etching and metallization. The presented techniques were developed in collaboration with Gisela Biehne (Universität Leipzig). An overview of the used photolithography templates is given in appendix A. In this chapter, the basics of photolithography and fabrication steps for MISFET, MESFET and inverters are given.

For the structuring of thin films with lithographic methods, light, x-rays or particles like electrons or ions are used. They give the ability to fabricate device structures in the scale of micrometer or sub micrometer. The fundamental advantage of lithography is the fabrication of a large number of copies from one original. With that, mass production in electronics became possible, leading to very low costs of one individual device.

In the lithographic process, certain areas of the sample are covered by a mask (e.g. a film of lacquer or a polymer, SiO_2, Si_3N_4, metalls), which has to be structured itself. Its properties are chosen with respect to the subsequent steps, e.g. regarding its chemical resistance or temperature sensitivity. The structuring process starts with the deposition of a radiation sensitive material, e.g. a lacquer mask is usually consisting of an organic polymer, which is designated as resist. The deposition is usually done by means of spin-coating. A distinction is drawn between positive and negative resists. For positive (negative) resists, the chemical solubility is increased (decreased) by radiation. The dissolution of certain areas of the resist is referred to as developing. After structuring of the lacquer mask, the laid open areas of the sample can be processed (e.g. metallized, oxidized, doped) or removed (e.g. wet-chemical etching, ion milling).

When visible or ultra-violet light is used for the structuring of the lacquer mask, the process is designated as photolithography. The used templates in this thesis consist of a $3 \times 3\,\text{inch}^2$ large and 2 mm thick quartz panel with an approximately 100 nm thick chromate absorbing layer. The templates are fabricated by *Rose Fotomasken, www.rose-fotomasken.de*. A mercury-vapor lamp, with its most intensive spectral lines at 436 nm, 405 nm and 365 nm, serves as light source. The exposition is differentiated between imaging systems (e.g. by mirrors or lenses) and the here used 1:1 shadow projection. If the template is pressed against the lacquor mask, the process is referred to as contact exposition; if there is a gap between template and sample, it is called proximity exposition (Fig. 3.3).

The resolution of the photolithography is limited by optical diffraction. For a given thickness s of the resist, a proximity distance d_{prox} and a wavelength λ, the minimal resolution is given by [Sin03]

$$b_{\text{min}} = \frac{3}{2}\sqrt{\lambda\left(d_{\text{prox}} + \frac{s}{2}\right)}\,. \tag{3.1}$$

With $\lambda = 436\,\text{nm}$, $s = 1\,\mu\text{m}$ and, for example, $d_{\text{prox}} = 20\,\mu\text{m}$, the minimal resolution is approximately $b_{\text{min}} \sim 4.5\,\mu\text{m}$; using contact exposition, it is $b_{\text{min}} = 0.7\,\mu\text{m}$. During this thesis, the smallest

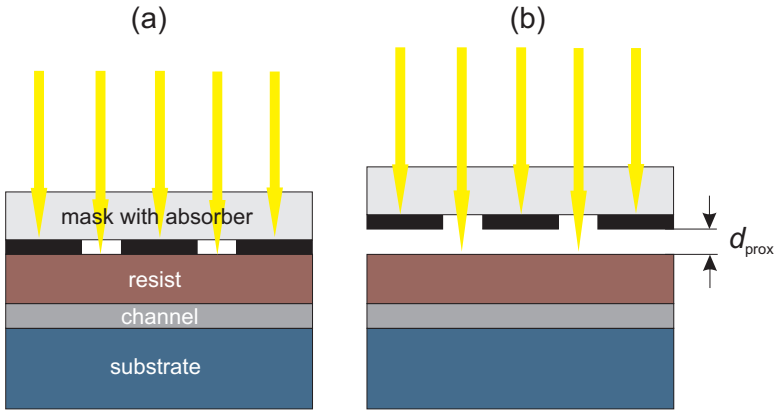


Figure 3.3: a) Contact and b) Proximity exposition of a resist in photolithography.

used dimension is 5 μm. Thus, using contact exposition, the reproducability of mask alignment is assured.

3.3.1 Photolithographic steps

The photolithography is done using a *SÜSS MJB3 Mask Aligner*. Each photolithographic step, i.e. each step using one template, is subdivided into: a) Deposition and structuring of the mask, b) Manipulation of the laid open surface, and c) Dissolution of the mask. These steps are explained in the following paragraphs.

Deposition and structuring of the mask

1. Typically, $10 \times 10\,\mathrm{mm}^2$ large samples are too small for the alignment table and have to be mounted with colophony on a piece of a larger substrate, e.g. GaAs or Si. Leftovers of the colophony are removed by acetone and the sample is dried in an oven (90°C, 5 min).
2. Spin-coating (4000 min^{-1}, 30 s) of the positive resist AZ1350H and drying in oven (90°C, 15 min).
3. Alignment of the template and exposition (7 s).
4. Developing of the mask using NaOH lye (6.64 g/l), washing in distilled water, spin-drying and drying in oven.

Manipulation of the laid open surface

This step is different for each device and template. It consists of the metalization using dc-sputtering, wet-chemical etching of the channel mesa structure using phosphoric acid (1:80, 20–25 s at room-temperature, etch-stop with water), or the PLD-growth of additional layers (e.g. TCO or insulator).

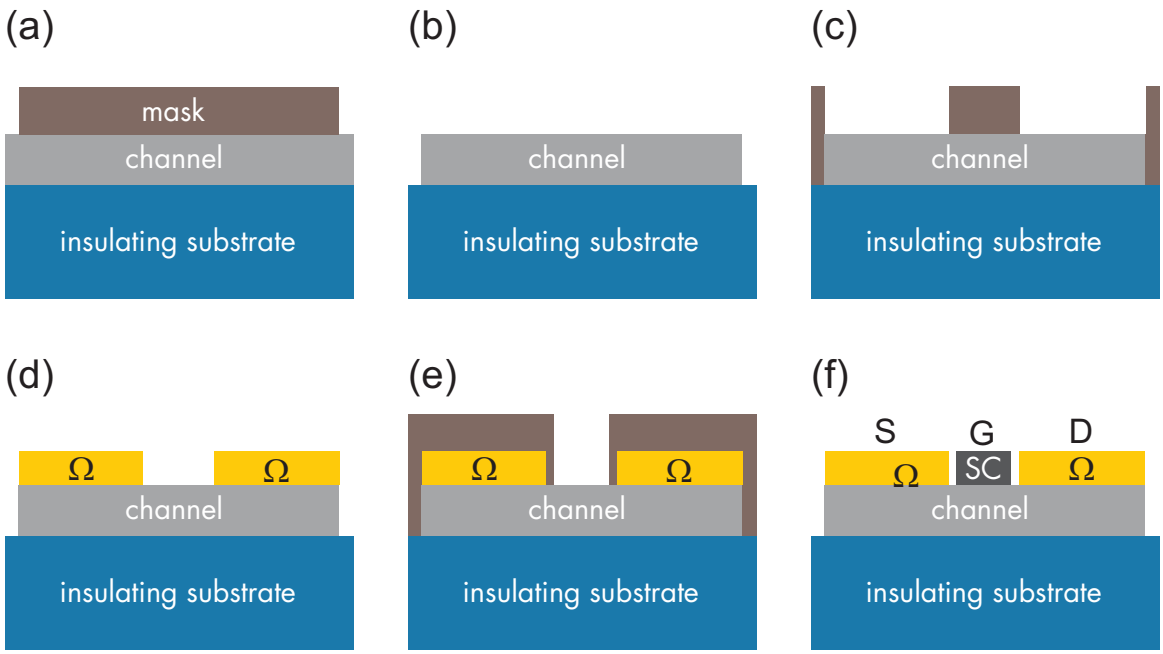


Figure 3.4: Scheme of the photolithographic fabrication process of a MESFET. a-b) mesa etching, c-d) deposition of source-drain contacts, e-f) deposition of the gate contact.

Dissolution of the mask

The dissolution of the mask (and the redundant metal or PLD-grown material) is done using acetone. The sample is first laid in acetone for one or more minutes to apply a little solvent to the mask, before the rest of the mask is dissolved within an ultrasonic bath. Thus it is ensured that the edges of the device are even and smooth.

A scheme of the photolithographic processing of a MESFET is depicted in Fig. 3.4. It consists of three steps. First, a mesa structure is wet-chemically etched into the ZnO to form channels ensuring that the current path will be directed straight from source to drain and crosstalk between different FET is excluded. Second, Au is dc-sputtered forming ohmic source and drain contacts. Third, the Schottky-gate contacts are reactively dc-sputtered.

The processing of a top-gate MISFET using a lift-off technique is depicted in Fig. 3.5. After wet-chemical etching of the mesa structure, the mask for the source-and drain contacts is used to deposit Au as sacrificial layer. This layer is non-reactively dc-sputtered for several minutes (instead of seconds, cmp. Sec. 3.2) such that its thickness is larger than that of the subsequently deposited insulator, e.g. $> 200\,\mathrm{nm}$. This ensures, that the sacrificial layer can later be attacked by the chemical-etch solution. Then, the insulator is grown by PLD with the parameters found in chapter 4. The use of Au as sacrificial layer has two advantages. First, it allows higher-temperature PLD-growth of insulators. Second, it can be removed using a selective etch-solution for Au (KI/I_2, $KI{:}I_2{:}H_2O$=4 g:1 g:40 ml) without attacking the ZnO layer. Then the template for source, drain and gate-contacts (cf. Appendix A) is used to deposit the ohmic contact metal.

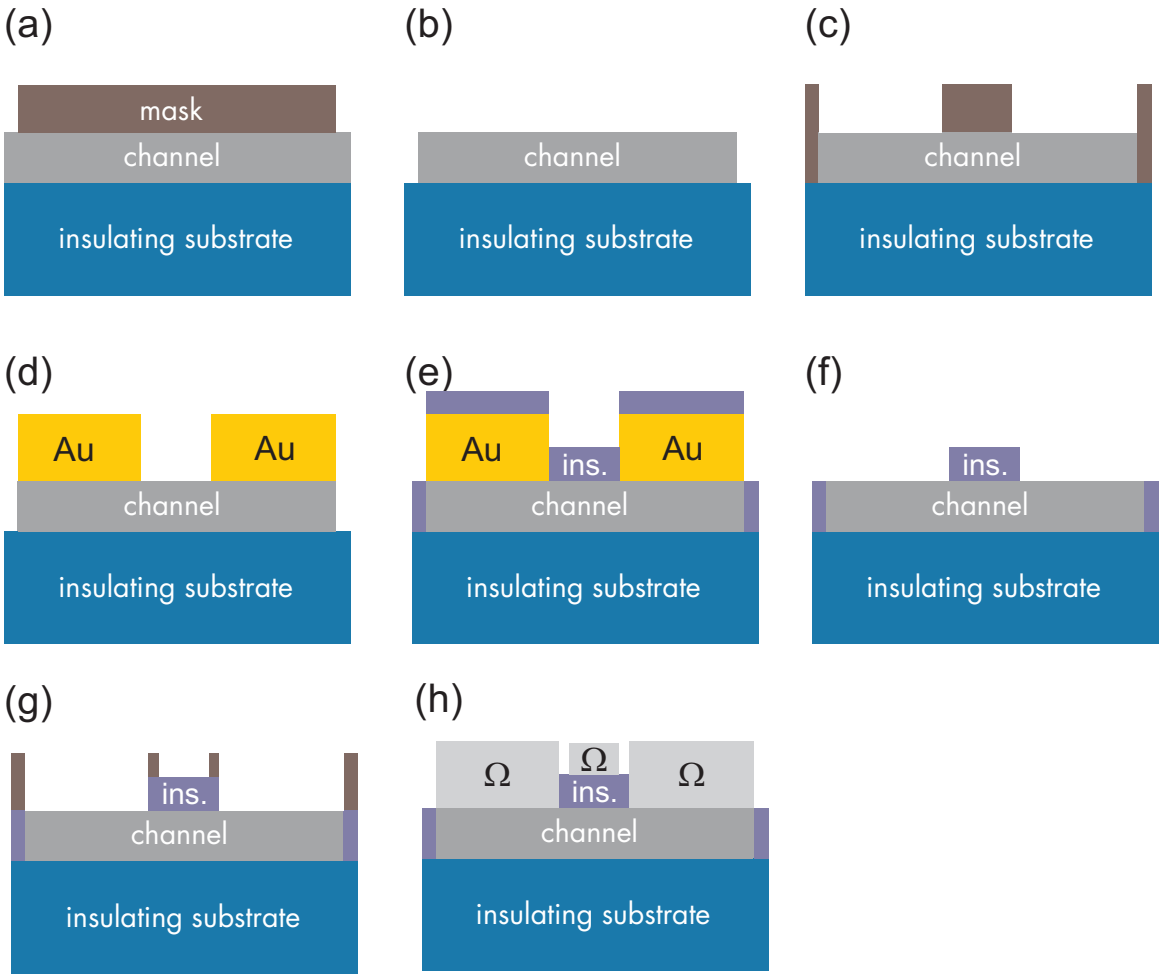


Figure 3.5: Scheme of the photolithographic fabrication process of a top-gate MISFET. a-b) mesa etching, c-d) deposition of Au sacrificial layer, e) PLD of insulator, f) lift-off of Au-layer, g-h) metalization.

The processing steps for the inverters are similar to that of the MESFET. However, they are different for the different types of inverters (Appendix A). The steps for the simple inverter are: alignment, mesa etching, deposition of the gate contact and deposition of ohmic contacts. The latter two steps are interchanged, because at the shortcircuit of source and gate of the load transistor, the ohmic metal has to be deposited on top of the capping layer of the Schottky contact. Otherwise, an ohmic-Schottky-ohmic junction would occur. For the FET-logic inverter, additional steps for the insulating cross-over and interconnections are needed (cf. Fig. A.4). The number of steps could be reduced for the SDFL-inverter, which has the same steps as the simple inverter or MESFET (cf. Fig. A.5).

3.4 Current-voltage measurement

The processed devices (MISFET, MESFET, inverter, MIS/MIM diodes) were measured (if not differently assigned) under dark conditions in ambient air and at room-temperature using an *Agilent*

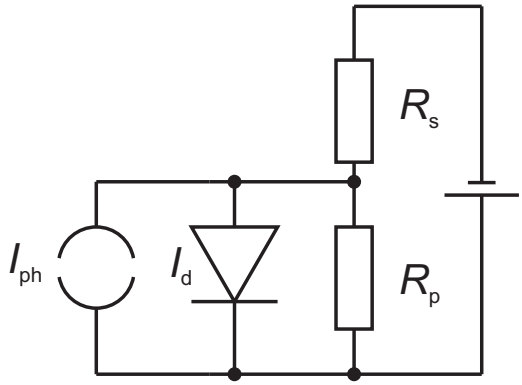


Figure 3.6: Equivalent circuit of a real Schottky diode with parallel resistance R_p, serial resistance R_s and photo-generated current I_{ph}.

4156C Precision Semiconductor Parameter Analyzer connected to a *SÜSS semi-automatic Waferprober* equipped with tungsten probes. The automation software "autoWP" for the Waferprober was written by Fabian Klüpfel (Universität Leipzig) on the basis of the measurement software of Matthias Brandt (Universität Leipzig). For the import and analysis of the measurement data, a script, developed by Tobias Dietz (Universität Leipzig), for *OriginPro 8G* was used.

3.4.1 Real Schottky diode

Using Eqns. 2.17 and 2.18 with the area of the Schottky contact and the equivalent circuit (Fig. 3.6), the real current-voltage characteristic of the Schottky diode is given by

$$I(V) = I_{sat}\left[\exp\left(\frac{q(V - IR_S)}{\eta k_B T}\right) - 1\right] + \frac{V - IR_S}{R_P}\,, \tag{3.2}$$

where R_S and R_P are the serial and parallel resistance, respectively. R_S limits the maximum current of the Schottky diode in forward direction and should be ideally zero. However, it is given by the conductivity of the semiconductor, the cross-section of the channel and the distance between the electrodes. Real values of R_S lie in the range of several kΩ. R_P, on the other hand, limits the current in reverse direction and should be ideally infinite. However, parasitic current paths, e.g. surface conduction, reduce R_P and thus decrease the rectification ratio of the diode, due to higher leakage currents.

3.4.2 Charge transport in real insulators

Real insulators are generally conducting at high temperatures and electric fields. Several mechanisms for that are considered in this section. Often, conduction mechanisms such as Poole-Frenkel and Schottky emission were reported for the insulators that are of interest in this thesis [Nan07, Cha01, Cha06]. However, not all mechanisms can be observed at the same time [Yan04], since some tend to dominate over the other at a certain voltage or temperature range [Mea62].

Under high electric field and low temperatures, tunneling is one of the commonly encountered transport processes and does basically not depend on temperature. It can be described by a wave function of electrons or holes which is able to penetrate the potential barrier. The process depends on the applied voltage and the thickness of the insulating film and can be expressed as ([Sze81])

$$J_{\mathrm{FN}} \propto \mathcal{E}_{\mathrm{i}} \exp\left(-\frac{4\sqrt{2m^*}(q\phi_{\mathrm{B}})^{3/2}}{3q\hbar\mathcal{E}_{\mathrm{i}}}\right), \tag{3.3}$$

where $\mathcal{E}_{\mathrm{i}} = \frac{V_{\mathrm{i}}}{d_{\mathrm{i}}}$ is the electric field in the insulator, m^* the effective mass and ϕ_{B} the barrier height. However, in this work, the common thickness of the insulator is of the order of 10^2 nm. Therefore, this mechanism is not expected.

At high electric fields and temperatures, Schottky emission (SE) is possible. This process is comparable to thermionic emission (cf. Sec. 2.1.3):

$$J_{\mathrm{SE}} \propto A^* T^2 \exp\left(\frac{-q(\phi_{\mathrm{B}} - \sqrt{q\mathcal{E}_{\mathrm{i}}/4\pi\epsilon_{\mathrm{i}}})}{k_{\mathrm{B}}T}\right), \tag{3.4}$$

where the barrier height is reduced due to image-force lowering (similar to the Schottky effect). A^* is the effective Richardson constant. A straight line is obtained from the plot of $\ln J/T^2$ over $1/T$ for this mechanism and the barrier height can be extracted from the slope.

Poole-Frenkel (PF) emission is observed at high temperatures and fields, where trapped electrons are emitted from the insulator into the conduction band of the semiconductor. The expression is similar to Eqn. 3.4 for Schottky emission

$$J_{\mathrm{PF}} \propto \mathcal{E}_{\mathrm{i}} \exp\left(\frac{-q(\phi_{\mathrm{B}} - \sqrt{q\mathcal{E}_{\mathrm{i}}/\pi\epsilon_{\mathrm{i}}})}{k_{\mathrm{B}}T}\right), \tag{3.5}$$

where ϕ_{B} is now the depth of the potential well of the traps. The reduction of this height is twice as large as compared to Schottky emission due to positive charges being immobile.

For high temperatures but low fields, an ohmic characteristic is observed. The electrons are thermally excited and hop from one isolated state into the other. The expression is exponentially dependent on the temperature

$$J_{\mathrm{Ohm}} \propto \mathcal{E}_{\mathrm{i}} \exp\left(-\frac{\Delta E_{\mathrm{ac}}}{k_{\mathrm{B}}T}\right), \tag{3.6}$$

with ΔE_{ac} being the activation energy for electrons.

A hysteresis obtained in IV measurements may result from ionic conduction. When a voltage is applied on the MIS diode, the potential distribution is altered. This is due to the built-up of space charges near the metal-insulator and insulator-semiconductor interfaces. An internal field remains

even after the applied voltage is turned off and some ions return to equilibrium. The expression is given by

$$J_{\text{ion}} \propto \frac{\mathcal{E}_{\text{i}}}{T} \exp\left(-\frac{\Delta E_{\text{ai}}}{k_{\text{B}} T}\right) , \tag{3.7}$$

where ΔE_{ai} is the activation energy for ions.

For very large electric fields, dielectric breakdown can occur as defects are caused by high energetic charge carriers. A breakdown path is created by the dense defects connecting the metal with the semiconductor within the insulating layer.

3.5 Capacitance-voltage measurement

CV measurements are used within this thesis for two purposes. On the one hand, the quasi-static CV (QSCV) measurement is used to determine the net doping concentration in the ZnO channel of MESFET and MIS-devices after Eqn. 2.8 and to determine the fixed and mobile charges in the non-ideal insulator of MIS-diodes from the flat-band voltage shift [Sze81]

$$V_{\text{FB}} - \phi_{\text{ms}} = -\frac{Q_{\text{f}}}{C_{\text{i}}} , \tag{3.8}$$

and from the hysteresis of the CV characteristic

$$V_{\text{FB}}(\text{forward}) - V_{\text{FB}}(\text{reverse}) = -\frac{Q_{\text{m}}}{C_{\text{i}}} . \tag{3.9}$$

On the other hand, frequency-dependent CV and admittance measurements are used to determine the interface trap density in MIS-diodes and Schottky-diodes.

3.5.1 Quasi-static capacitance-voltage measurement

The QSCV measurements were carried out with the *Agilent 4156C Precision Semiconductor Parameter Analyzer*. In this measurement mode, a linear staircase voltage sweep is performed [Agi08]. Around each measurement step, a voltage sweep ΔV is performed; the voltage and the current is measured and the capacitance is calculated by

$$C = \frac{I t_{\text{int}}}{\Delta V} , \tag{3.10}$$

where t_{int} is the integration time of the measurement. Additionally, the leakage current I_{L} at each step is measured and subtracted from I, i.e. $I = I - I_{\text{L}}$. Before the measurement, the zero capacitance, i.e. the capacitance of the setup including measurement device, waferprober and cables, is measured and

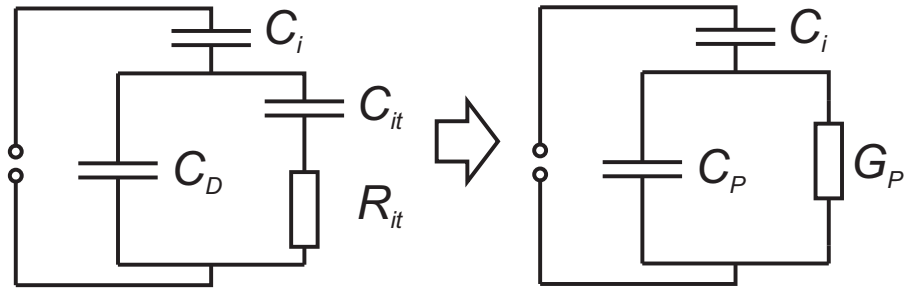


Figure 3.7: Equivalent circuit of the MIS diode (left) and for the conductance measurement of the MIS diode (right).

is used for correction of the later measured capacitance. The measurement time for one point lies in the range between 0.04 s and 400 s. The maximum frequency is ~25 Hz, which is very low compared to the frequency range of the standard CV measurement (40 Hz–10 GHz). With that, all charges can follow the measurement frequency.

Due to the insulator, the QSCV measurements of the MIS-diodes are very accurate, because only low leakage current (below 1 nA) flows over a wide voltage range. For the MESFET, due to the thin channel layer and the Schottky-gate, the QSCV measurements are only valid in a small voltage range around $V_G = 0$, where the depletion layer can still be varied by a voltage and does not hit the insulating substrate and where the leakage current is low enough to ensure the leakage current compensation. For this reason, the determination of $N_D - N_A$ from only one measurement is not very reliable. Instead, five to ten QSCV measurements were performed for different MESFET devices on one substrate to find a more accurate mean value for the net doping concentration.

3.5.2 Admittance spectroscopy

Admittance spectroscopy measurements (AS) were carried out on socketed samples using the *Agilent 4294 Precision Impedance Analyzer*. For that the samples (MIS- or Schottky-diodes) were mounted on TO-32 sockets and connected using gold wires and conducting epoxy resin. The interface trap charges of MIS-diodes are distributed across the energy bandgap, their density is given by [Sze81]

$$D_{it} = \frac{1}{q}\frac{dQ_{it}}{dE} . \tag{3.11}$$

When a voltage is applied, the energy bands and interface-trap levels are bent with respect to the Fermi energy level, which results in a charge or discharge of the interface traps. This can be measured using an equivalent circuit for the MIS diode (Fig. 3.7), where the insulator capacitance C_i and the depletion layer capacitance C_D are connected in series, whereas the capacitance C_{it} and resistance R_{it} of the interface traps are connected parallel to C_D. The product $\tau = R_{it}C_{it}$ is the interface trap lifetime. This circuit can be considered as a parallel circuit of a capacitance C_P and a conductance G_P that both depend on the frequency ω as

$$C_P = C_D + \frac{C_{it}}{1+\omega^2\tau^2} \tag{3.12}$$

$$\frac{G_P}{\omega} = \frac{C_{it}\omega\tau}{1+\omega^2\tau^2}. \tag{3.13}$$

Therefore, plotting G_P/ω versus ω, the maximum value is where $\omega\tau = 1$ and $G_P/\omega = C_{it}/2$. The interface trap density can then be obtained by

$$D_{it} = \frac{C_{it}}{qA}\ , \tag{3.14}$$

where A is the contact area. Combining QSCV measurements with this conductance measurements using V_G as parameter, the surface potential can be obtained by

$$\psi_s(V_1) - \psi_s(V_2) = \int_{V_2}^{V_1} \left(1 - \frac{C}{C_i}\right) dV\ . \tag{3.15}$$

With $E = q\psi_s - E_G/2$, the interface trap density can then be plotted as a function of energy within the energy bandgap.

4 Pulsed-laser deposited insulators and metal-insulator field-effect transistors

This chapter covers the properties of insulators that were grown by pulsed-laser deposition (PLD) and metal-insulator-semiconductor field-effect transistors (MISFET) based thereon. The measurements were performed in collaboration with Nuchjarim Yensuong (Universität Leipzig) within the scope of her master thesis [Yen09]. In the first instance, single-layer high-κ insulators ZrO_2 and HfO_2 are considered. Some properties of various insulators are given in Tab. 4.1. There is a trade off between the dielectric constant κ and the energy bandgap. On the one hand, large κ-values are needed to obtain high insulator capacitances, which allow to reduce the thickness of the insulator. On the other hand, large bandgaps and with that large conduction-band offsets to the semiconductor are needed in order to minimize electron injection into the insulator bands. For the sake of low-power operation, the thickness of the insulator should be at most 100 nm. To combine both high-κ and band offset, sandwich structures, where ZrO_2 or HfO_2 are sandwiched between two layers of Al_2O_3 [Din07], are also considered. Within these structures, the band offsets between ZnO, Al_2O_3, and HfO_2/ZrO_2 form a barrier for electrons.

For two reasons, the insulators should be grown at low temperatures: a) to avoid decomposition of the photo resist (which is stable at temperatures below 90°C), a room-temperature PLD process is recommended for the fabrication of the top-gate contacts, b) for low-temperature growth, most oxide insulators become amorphous [Jeo05]. The disordered structure of amorphous oxide insulators reduces the probability of current paths through the insulator film. Nevertheless, the following investigations include various growth temperatures between 25°C and 580°C (corresponding to substrate heater powers between 0 W and 500 W). Wide-angle X-ray-diffraction (XRD) 2θ-ω scans show (Fig. 4.1a), that the intensity of the (-111) peak of monoclinic ZrO_2 decreases with the decreasing growth temperatures during the PLD process. This indicates a reduced crystallinity of the sample. The same behavior can be observed for HfO_2 (Fig. 4.1b), where the (-111) peak completely vanishes for room-temperature growth; the HfO_2 film is amorphous and should therefore lead to higher insulation.

Table 4.1: Properties of various insulators [Rob06] in comparison with ZnO.

Material	dielectric constant κ	Bandgap (eV)
ZnO	8.12	3.4
Al_2O_3	9	8.8
HfO_2	25	5.8
ZrO_2	25	5.8
MgO	10	7.6

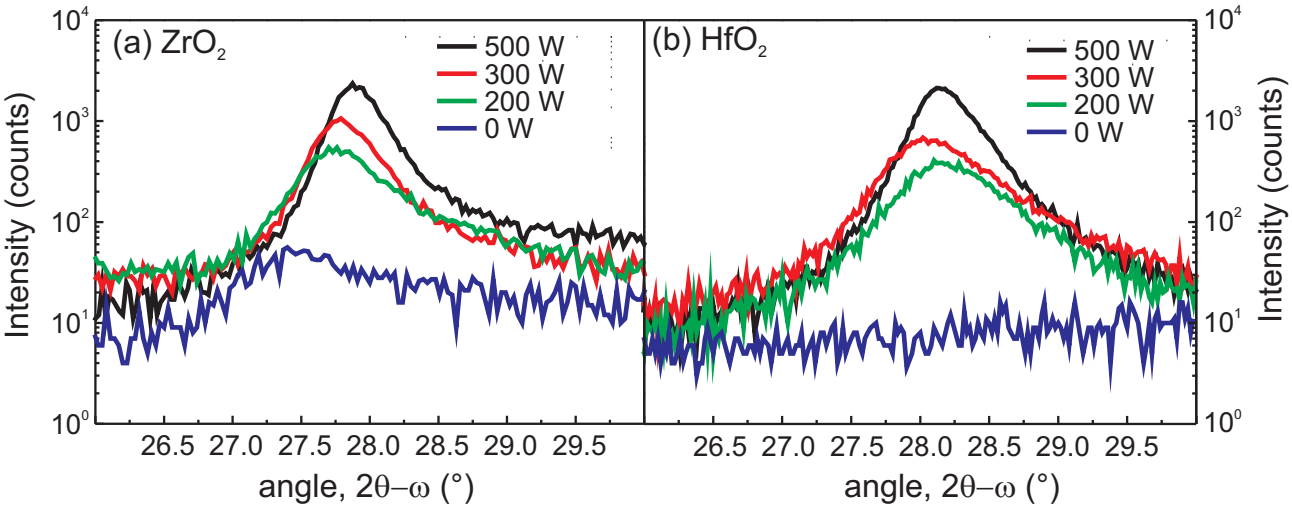


Figure 4.1: XRD 2θ-ω scans of the (-111) peak of a) ZrO_2 and b) HfO_2 in MIS structures grown with various heater powers.

4.1 Metal-insulator-metal structures

First, the insulators are investigated in simple metal-insulator-metal (MIM) capacitors. Within this structure, the insulator is grown on top of either a metal or degenerately Al-doped (metallic conducting) ZnO. A scheme of the used MIM structure is shown in Fig. 4.2b; the MIS structure is depicted in Fig. 4.2a. The back contact is connected using Au, dc-sputtered on the corners of the $10 \times 10\,mm^2$ samples [Wen06]. As ohmic front contact, dc-sputtered Pt was deposited through shadow masks, leading to circular contacts with areas between $4 \times 10^{-4}\,cm^2$ and $4.9 \times 10^{-3}\,cm^2$. After deposition, the Pt contacts were annealed at 500–600°C for 30 minutes in 700 mbar oxygen atmosphere. This leads to an out-diffusion of the Pt from the insulating layer resulting in a sharp and abrupt interface.

Room-temperature current-voltage (RT-IV) measurements were used for the classification into "insulating" and "not-insulating". The dielectric constants κ are obtained from QSCV measurements and compared to the literature. The possible origin of conduction through the insulators is investigated by means of temperature-dependent IV measurements.

4.1.1 Current-voltage measurements

The insulator thickness of the ZrO_2 and HfO_2 MIM capacitors is set to approximately 150 nm. It was measured either using spectroscopic ellipsometry performed by the ellipsometry workgroup at Universität Leipzig, or, for selected samples by cross-section field-emission microscopy performed by Jörg Lenzner (Universität Leipzig). IV characteristics were measured in the voltage range of ±1 V, where the positive electrode was set to the Pt contact. Figure 4.3 depicts typical IV characteristics of MIM capacitors using ZrO_2 and HfO_2. The majority of the samples shows forward conduction. The increase of the current typically starts in a voltage range between 0.1 V and 0.3 V. the possible origin of this conduction is investigated in Sec. 4.1.3 by means of temperature-dependent IV-measurements.

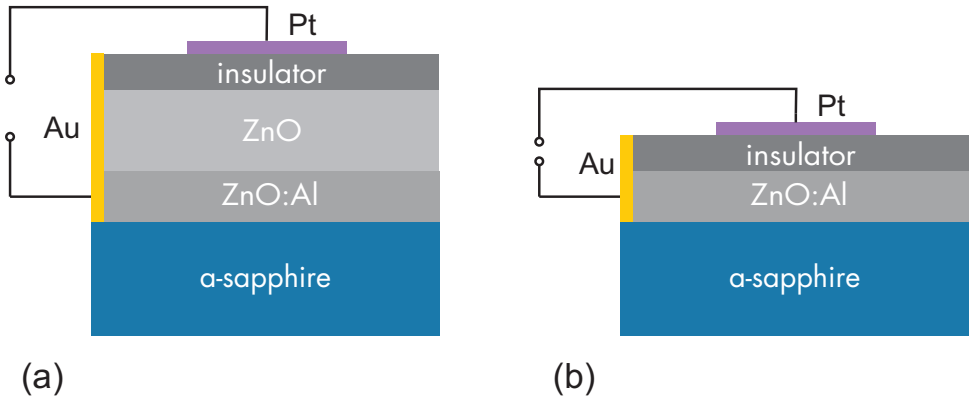


Figure 4.2: Scheme of a a) MIS structure and b) MIM structure.

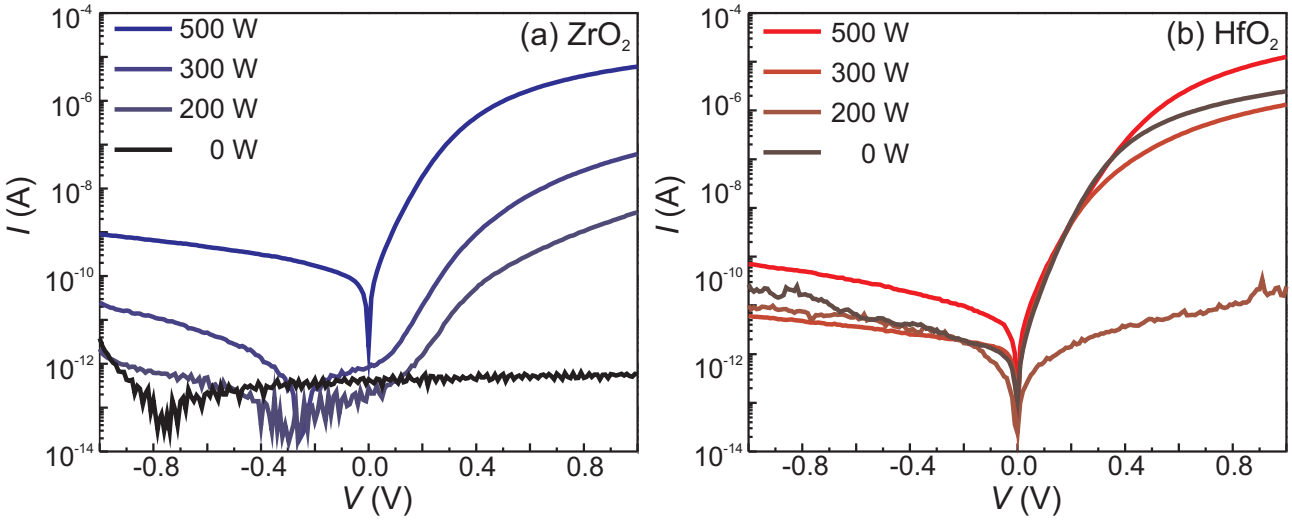


Figure 4.3: Typical IV characteristics of MIM capacitors with a) ZrO_2 and b) HfO_2 as insulating layer.

The IV measurements are statistically analyzed by means of histograms, which show the relative frequency of contacts having leakage current densities in given classes of ranges. Contacts with leakage currents below 10^{-10} A or 10^{-6} Acm^{-2} are defined to be insulating. Figure 4.4a-d depicts the histograms for ZrO_2 and HfO_2, respectively. In each case, the leakage currents at −1 V and +1 V are plotted for various substrate heater powers during PLD growth of the insulator. In Refs. [Kim04, Chi03], the crystalline state of the insulator is reported to be affected by the substrate temperature. It is clearly preferable to use an insulator in the amorphous state inorder to reduce leakage currents that come from conducting paths along grain boundaries. According to Fig. 4.1, the 0 W samples should have the lowest leakage currents. For ZrO_2 (Fig. 4.4a,b), the 0 W sample has 81% insulating contacts at −1 V. At +1 V, only 40% of the contacts are insulating. However, the 0 W sample has the highest frequency of insulating contacts, whereas e.g. the 500 W sample has only 70% at −1 V and no insulating contact points at +1 V. For HfO_2 (Fig. 4.4c,d), the relationship between substrate heater power and insulating contacts is not as clear as for ZrO_2. Generally, it shows higher leakage currents compared to ZrO_2. The MIM capacitor grown at 0 W has more than 90% of the contacts in the non-

Table 4.2: Mean dielectric constants of insulators in MIM structures.

insulator	d (nm)	C_i (10^{-7}Fcm^{-2})	κ	κ from ref.
ZrO_2	204	1.08	24.8	20–25 [Kim04]
HfO_2	110	1.01	12.5	13–16 [Hon04]
Al_2O_3–ZrO_2–Al_2O_3	104	1.73	20.2	–
Al_2O_3–ZrO_2–Al_2O_3	245	0.74	20.5	–
Al_2O_3–HfO_2–Al_2O_3	82	2.22	20.6	7.2 [Che05]
Al_2O_3–HfO_2–Al_2O_3	189	0.72	15.4	–

insulating regime for both voltage directions. Here, the 200 W sample has most of the contacts (58%) in the insulating regime for −1 V, but almost no contact for +1 V.

As the single-layer insulators did not show a sufficient insulating behavior, sandwich structures as reported in [Che05, Din07, Cha08] are considered. In this structures, the high-κ insulators ZrO_2 of HfO_2 are grown between layers of Al_2O_3. Having a larger bandgap of 9 eV, the Al_2O_3 layer provides a larger barrier for electrons and an additional barrier for diffusion of metals from the electrodes. On the other hand, the lower κ-value of Al_2O_3 is compensated by the ZrO_2 and HfO_2. The overall κ-value can be determined considering the sandwich structure as series of capacitances [Che05]

$$C_i^{-1} = 2\frac{d_{Al_2O_3}}{\kappa_{Al_2O_3}} + \frac{d_{ZrO_2/HfO_2}}{\kappa_{ZrO_2/HfO_2}} = \frac{2d_{Al_2O_3} + d_{ZrO_2/HfO_2}}{\kappa_{avg}}\,, \tag{4.1}$$

where κ_{avg} is the average dielectric constant of the whole sandwich insulator.

Figure 4.4e,f depicts the histograms for Al_2O_3–ZrO_2–Al_2O_3 and Al_2O_3–HfO_2–Al_2O_3 sandwich insulators for various overall thicknesses. The thickness of the ZrO_2 and HfO_2 was kept constant, whereas the thickness of the Al_2O_3 layers is doubled. It is obvious, that the leakage current suppression is more effective for the sandwich insulators compared to the single-layer insulators. Even the thinner insulators have nearly 100% insulating contact points at −1 V and 90% at +1 V for the ∼ 104 nm thick ZrO_2-sandwich as well as 92% (−1 V) and 100% (+1 V) for the ∼ 82 nm HfO_2-sandwich, respectively. However, also for the sandwich samples, HfO_2 has higher leakage currents than ZrO_2.

4.1.2 Quasi-static capacitance-voltage measurements

Those samples, which have shown a stable insulating behavior were investigated by QSCV measurements. For the sandwich structures, the contacts showed a constant capacitance up to a voltage of −20 V. The ZrO_2 and HfO_2 single layers had a constant capacitance up to −6 V and −4 V, respectively. For larger negative voltages, the leakage current increases drastically and could not longer be compensated by the QSCV set-up. The dielectric constants κ were obtained from the insulator capacitance C_i and the mean values (averaged over all insulating contacts) are listed in Tab. 4.2.

On the one hand, the mean κ-value of 24.8 for ZrO_2 is comparable to the values for bulk ZrO_2 from the literature (κ = 20–25 [Kim04]). On the other hand, the mean κ = 12.5 for HfO_2 is lower than

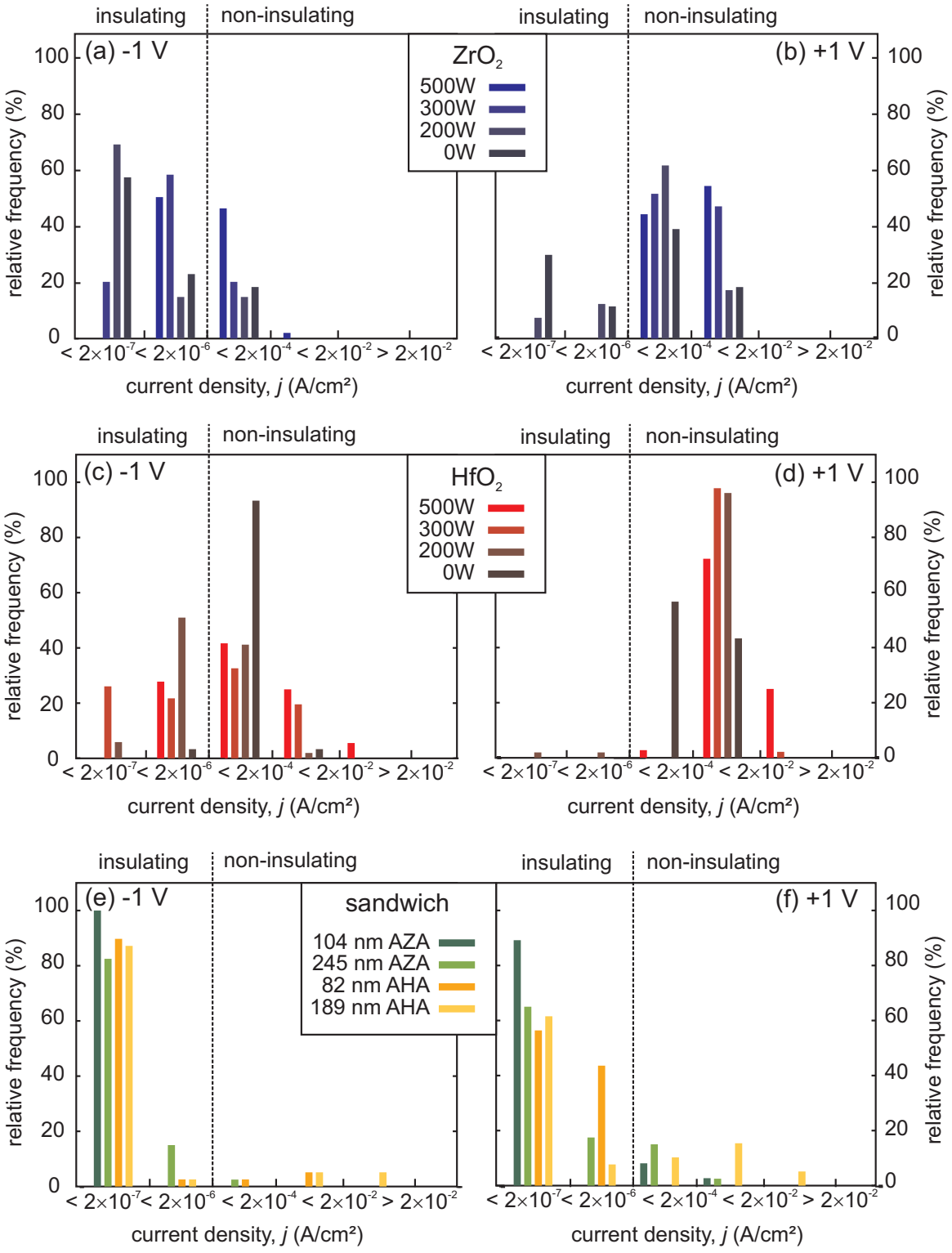


Figure 4.4: Histograms of the leakage current for MIM capacitors using a-b) ZrO_2, c-d) HfO_2 and e-f) sandwich-structure insulators grown at different substrate heater powers (a-d) and with different thicknesses (e-f) at −1 V (a,c,e) and +1 V (b,d,f). (AZA: Al_2O_3–ZrO_2–Al_2O_3, AHA: Al_2O_3–HfO_2–Al_2O_3)

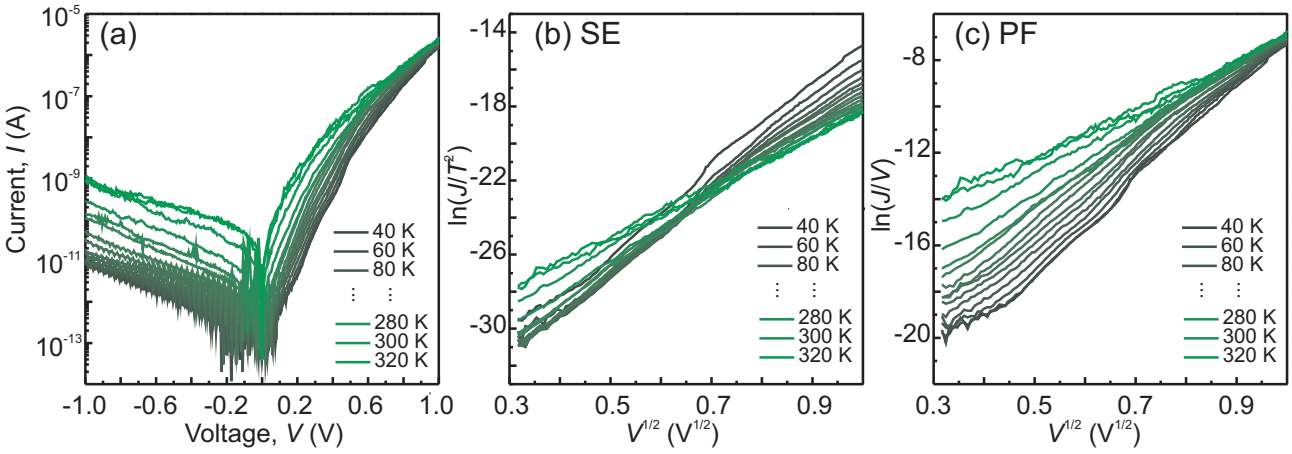


Figure 4.5: a) IVT-measurements of an Al_2O_3–ZrO_2–Al_2O_3 sandwich-structure MIM capacitor. b) Corresponding plot for Schottky emission (SE) and c) plot for Poole-Frenkel emission (PF).

e.g. reported in [Ahn06b] (κ = 20–25). However, there are reports having similar values around 13–16 [Hon04]. The lower κ-values indicate an incorrect stoichiometry of the insulator. For the sandwich structures, the lower $\kappa \sim 20$ is due to the low $\kappa \sim 9$ of Al_2O_3, which predominates the capacitance (Eqn. 4.1).

4.1.3 Temperature-dependent current-voltage measurements

Two MIM samples with an Al_2O_3–ZrO_2–Al_2O_3 sandwich insulator and a HfO_2 (300 W) single-layer insulator were investigated by means of temperature-dependent current-voltage measurements (IVT). For each sample, contacts with forward conduction were chosen and the samples were mounted and connected to TO-32 sockets. Both samples showed similar IV characteristics. Figure 4.5a depicts IV characteristics of an Al_2O_3–ZrO_2–Al_2O_3 sandwich structure in a temperature range between 40 K and 320 K. As expected, the leakage current increases with increasing temperature. This raw-data has been plotted in dependence of the temperature and electric field according to the relations given in Sec. 3.4.2. Only the plots for Poole-Frenkel (PF) emission and Schottky emission (SE), given in Fig. 4.5b and c, did show a linear behavior with positive slopes as expected from Eqns. 3.4 and 3.5. Therefore, PF and SE are the dominant conduction mechanisms in the PLD-grown insulators, whereas Fowler-Nordheim (FN) tunneling, Ohmic and ionic conduction can be excluded.

From Eqns. 3.4 and 3.5, the difference between the slopes should be a factor of 2:

$$D_{\mathrm{SE}} = \frac{q}{k_{\mathrm{B}}T}\sqrt{\frac{q}{4\pi\epsilon_{\mathrm{i}}d}} \tag{4.2}$$

$$D_{\mathrm{PF}} = \frac{2q}{k_{\mathrm{B}}T}\sqrt{\frac{q}{4\pi\epsilon_{\mathrm{i}}d}}. \tag{4.3}$$

Using these equations, the SE and PF slopes were calculated with the κ-value obtained from QSCV-

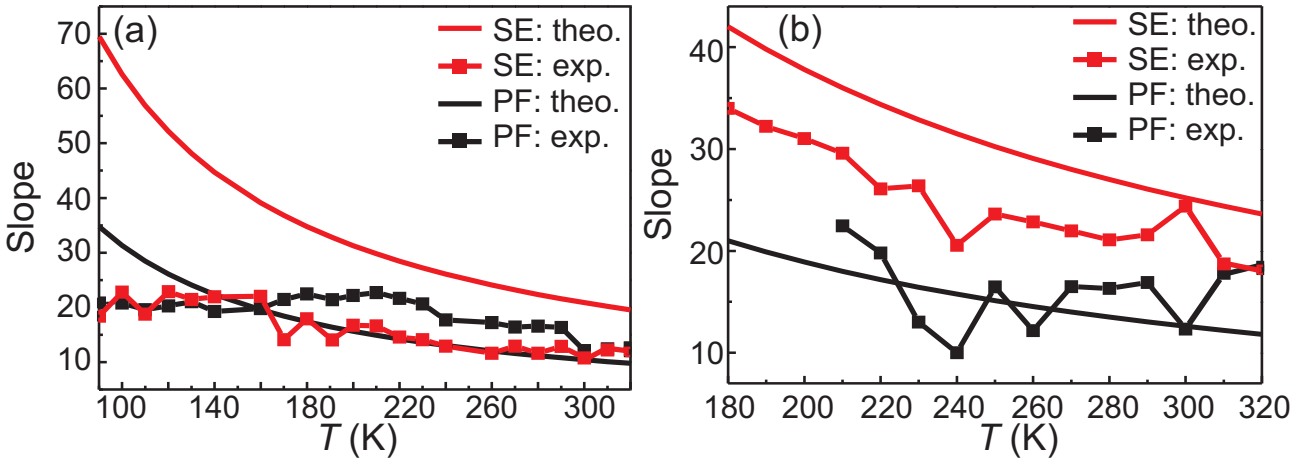


Figure 4.6: Plot of experimental and calculated slopes for Schottky emission and Poole-Frenkel emission for a) Al_2O_3–ZrO_2–Al_2O_3 and b) HfO_2 MIM capacitors.

measurement and the thickness obtained from cross-section FEM pictures. The calculated slopes are plotted in Fig. 4.6 together with the experimental slopes obtained from fitting the plots in Fig. 4.5b and c. For the ZrO_2 sandwich structure (Fig. 4.6a), only the SE values are close to the theoretical values, indicating, that SE is a probable conduction mechanism. The factor of 2 between SE and PF slopes is not observed for any temperatures. For the HfO_2 MIM capacitor (Fig. 4.6b), also the SE is appropriate. However, the PF values are closer to the theoretical characteristic. The factor of 2 is only observed for the room-temperature measurement, where both SE and PF mechanisms seem to be present.

4.2 Metal-insulator-semiconductor structures

The investigation of MIM capacitors showed, that PLD-grown ZrO_2 and HfO_2 are in principle capable as high-κ insulators. They exhibit low leakage currents and high κ-values that are similar to other reported ZrO_2- and HfO_2-layers, grown e.g. by molecular beam epitaxy [Hon04, Kim04]. However, the forward conduction of these insulators is the major concern. The application of sandwich-structure insulators using Al_2O_3–ZrO_2–Al_2O_3 and Al_2O_3–HfO_2–Al_2O_3 led to lower leakage currents but comparably high κ-values, making these structures promising for the use as gate-insulators in MISFET. The next step towards MISFET is the investigation of MIS-diodes by growing the insulators directly on the semiconducting ZnO. The influence of ZnO on the leakage currents and interface effects will be studied in this section.

4.2.1 Current-voltage measurements

Figure 4.7a,d depicts histograms of leakage currents at ±1 V for ZrO_2-ZnO and HfO_2-ZnO MIS diodes, for which the insulator is grown at various substrate heater powers. In contrast to the MIM structures, ZrO_2 and HfO_2 show similar behavior, indicating that the shortcoming of HfO_2 compared

Table 4.3: Properties of ZrO_2-ZnO MIS diodes obtained from QSCV measurements.

P_{heater} (W)	C_i (10^{-7}Fcm^{-2})	κ	N_D (10^{17}cm^{-3})	V_{FB} (V)	ΔV_{FB} (V)	N_f (10^{12}cm^{-2})	N_m (10^{10}cm^{-2})
500	2.17	33.9	1.53	-0.03	2.31	3.19	17.6
300	2.82	31.3	1.00	-0.75	3.02	5.33	17.6
0	1.48	20.8	0.29	-0.63	2.87	2.66	4.62

to ZrO_2 does not exist on ZnO. This is the expected behavior for these similar materials. However, the IV measurements still show forward conduction. Whereas, in reverse direction, the insulating behavior is more distinctive for the MIS diodes. A possible explanation is the depletion of the *n*-type ZnO for negative gate voltage. The electrons are kept away from the semiconductor-insulator interface. Hence, low leakage current is observed. When positive bias is applied, electrons accumulate at the interface forming a conductive layer; the leakage current increases for positive voltages. A clear relationship between leakage current and substrate heater power during PLD growth is not distinctive from the IV measurements. However, the 0 W HfO_2 MIS diode has 94% insulating contacts for −1 V, but only 12% for +1 V. As shown in Fig. 4.7e,f, the sandwich-structure insulators in MIS diodes are more insulating compared to single-layer insulators. There are more contacts with lowest leakage currents of 10^{-9} Acm^{-2} in both voltage directions. For the 90 nm thick Al_2O_3–HfO_2–Al_2O_3, 89% of the contacts are insulating in reverse direction and still 50% in forward direction. However, this is less than for the MIM capacitors. Even the sample with the thickest oxide (540 nm), where the second Al_2O_3 layer is three times thicker than the first, has 100% insulating contacts for −1 V but only 78% for +1 V. In this case, the sandwich structures with HfO_2 have lower leakage currents than that with ZrO_2.

4.2.2 Capacitance-voltage measurements

QSCV measurements of samples grown using various heater powers are given in Figs. 4.8a and b. The characteristics show, as expected for ZnO, deep-depletion behavior (cf. Sec. 2.2.2). With increasing heater power, the curves are more stretched out along the voltage axis, as the net doping concentration increases due to diffusion of Al from the backcontact and the substrate [Wen07a]. The QSCV curves for sandwich-structure MIS diodes are presented in Fig. 4.8c. The slopes in the depletion region are similar for all sandwich structures as the doping concentration is of the same magnitude of 10^{16} cm^{-3}. Note, that the large thickness of the 540 nm sandwich insulator MIS diode causes a large shift in flatband voltage. Therefore, the depletion cannot be observed within the breakdown limit of this device.

The Tables 4.3, 4.4 and 4.5 summarize the average values for the insulator capacitance C_i, the dielectric constant κ, the doping concentration N_D obtained from Eqn. 2.8, the flatband voltage V_{FB} and its shift ΔV_{FB} as well as the fixed and mobile insulator charges N_f and N_m calculated using Eqns. 3.8 and 3.9, obtained and extracted from the QSCV measurements of the ZrO_2, HfO_2 and sandwich-structure MIS diodes.

The κ-values for ZrO_2 and HfO_2 are decreasing with decreasing heater power due to lower crystallinity. Their mean values are higher than for the MIM capacitors and higher than other reported

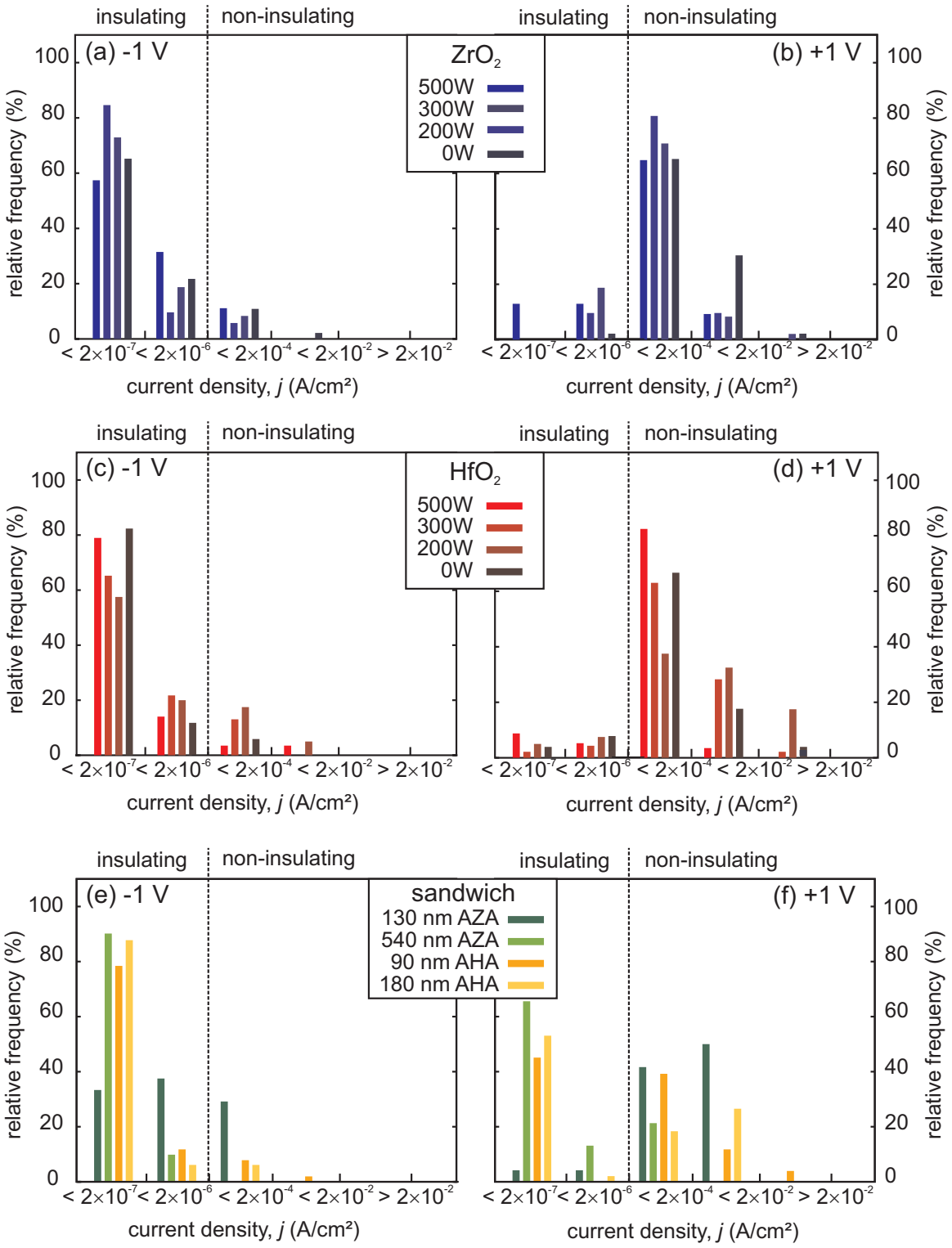


Figure 4.7: Leakage-current histograms for a-b) ZrO_2-ZnO, c-d) HfO_2-ZnO, and e-f) sandwich-structure MIS diodes at −1 V (a,c,e) and +1 V (b,d,f). (AZA: Al_2O_3–ZrO_2–Al_2O_3, AHA: Al_2O_3–HfO_2–Al_2O_3)

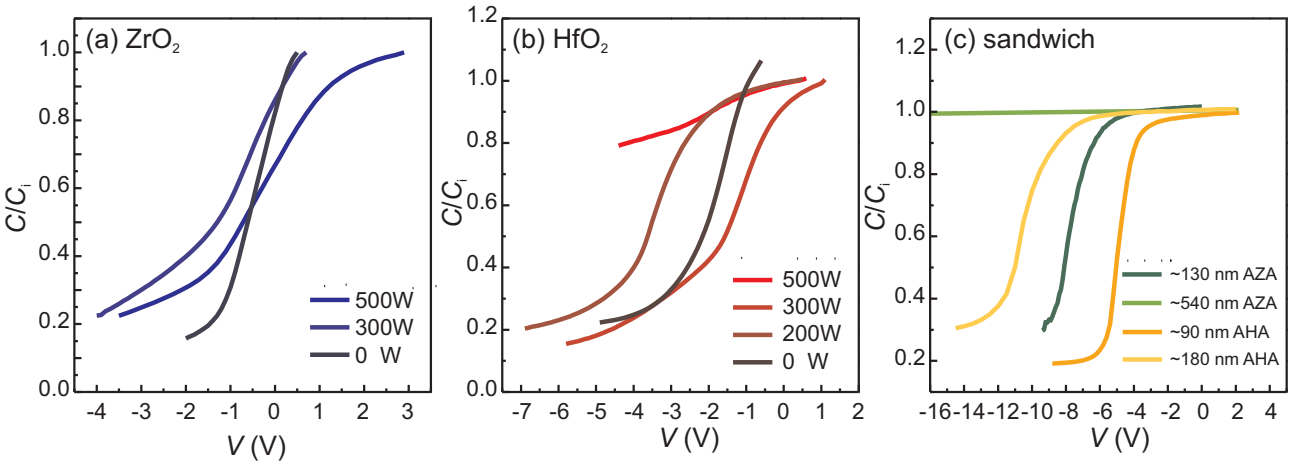


Figure 4.8: QSCV measurements of a) ZrO_2-ZnO, b) HfO_2-ZnO and c) sandwich-structure MIS diodes with various heater powers (a,b) and thicknesses (c).

Table 4.4: Properties of HfO_2-ZnO MIS diodes obtained from QSCV measurements.

P_{heater} (W)	C_i (10^{-7}Fcm^{-2})	κ	N_D (10^{17}cm^{-3})	V_{FB} (V)	ΔV_{FB} (V)	N_f (10^{12}cm^{-2})	N_m (10^{10}cm^{-2})
500	1.77	32.6	45.8	-1.08	3.46	4.14	8.84
300	1.96	25.9	0.63	-1.06	3.31	4.06	8.56
200	1.43	24.2	0.53	-2.82	5.06	4.18	4.46
0	1.49	20.8	0.45	-1.38	3.63	3.38	7.44

experimental values ($\kappa \sim 13$–21) [Cha01, Cho02, Chi03]. However, these reports often use Si as semiconductor, which forms an interface layer of zirconium silicate ($ZrSi_xO_y$) and thus reduces the dielectric constant. The sandwich insulators have lower κ-values in the range of 15 compared to the single-layer insulators as shown for the MIM capacitors. However, the mean κ-values for the MIS diodes are lower than for the MIM structures.

V_{FB} is shifted in the negative direction for all insulators. Positive fixed oxide charges Q_f were calculated and lie in the range of $N_f \sim 10^{12}$ cm^{-2}, which is comparable to other reports [Cha01]. The fixed oxide charge is typically positive due to an excess of metal in the insulator [Sze81]. There was

Table 4.5: Properties of sandwich-insulator MIS diodes obtained from QSCV measurements.

$Al_2O_3 - ZrO_2 - Al_2O_3$							
d (nm)	C_i (10^{-7}Fcm^{-2})	κ	N_D (10^{17}cm^{-3})	V_{FB} (V)	ΔV_{FB} (V)	N_f (10^{12}cm^{-2})	N_m (10^{10}cm^{-2})
128	1.08	15.5	0.29	-7.15	9.39	6.30	0.67
540	0.24	–	–	–	–	–	–
$Al_2O_3 - HfO_2 - Al_2O_3$							
90	1.44	14.7	0.41	-4.90	7.15	6.45	0.90
178	0.74	14.9	0.54	-9.80	12.04	5.53	4.61

no clear relationship between the substrate heater power and the flatband-voltage shift. Larger ΔV_{FB} were obtained for the sandwich structures compared to the single-layer structure. There was also a larger amount of fixed oxide charges, which may be due to the larger number of burried interfaces overall containing more traps. On the other hand, the sandwich structures have less mobile charges N_m compared to the single-layer insulators, which results in lower hysteresis.

Interface traps have been investigated by means of admittance spectroscopy. As for the QSCV measurements, low leakage currents for the negative and the positive voltage range are required. Figure 4.9a, c and e show admittance measurements for various voltages. With increasing voltage, the conductance peak shifts towards higher frequencies. The interface trap charge density D_{it} and time constant τ were determined as described in Sec. 3.5.2. For all insulators, no maximum of D_{it} was observed within the obtained energy range. That means, there are no discrete energy levels of interface traps but a continuum in the band gap. The obtained range of D_{it} lies between 7×10^{10} and 1×10^{11} cm^{-2}eV^{-1} for ZrO_2, 1×10^{11}–7.5×10^{11} cm^{-2}eV^{-1} for HfO_2 and 4.5×10^{11}–6.5×10^{11} cm^{-2}eV^{-1} for the 90 nm HfO_2 sandwich sample. These are typical values for high-κ insulators which lie in the range of 10^{11}–10^{12} cm^{-2}eV^{-1} [Wil01, Cha01, Chi03, Nan07]. The interface trap lifetime τ decreases with increasing energy, which is typical for *n*-type semiconductor MIS diodes, where the interface traps are usually acceptor-like [Ber06]. Furthermore, the range of τ decrases from 10^{-3}–10^{-4} s^{-1} for ZrO_2, over 10^{-4}–10^{-5} s^{-1} for HfO_2 to the range of 10^{-5}–10^{-6} s^{-1} for the HfO_2-sandwich structure. This coincides with the increase of D_{it} from ZrO_2 to the HfO_2-sandwich; i.e. τ decreases with increasing D_{it} and D_{it} increases for energies closer to the conduction-band edge.

In conclusion, high-κ insulators were grown by PLD. ZrO_2, HfO_2 and the sandwich structures Al_2O_3–ZrO_2–Al_2O_3 and Al_2O_3–HfO_2–Al_2O_3 were considered. All insulators showed sufficient insulating behavior for negative voltages, but forward conduction occured for positive voltages. However, the sandwich structures exhibit much lower leakage currents than the single-layer insulators because the Al_2O_3 serves as diffusion and electronic barrier. The dielectric constants of the insulators are similar to other reported values. The κ-values for single-layer insulators in ZnO MIS diodes were higher than that in MIM-capacitors. IVT measurements revealed, that Fowler-Nordheim tunneling, ohmic and ionic conduction can be excluded as possible conduction mechanisms. Instead, Poole-Frenkel and Schottky emission mechanisms are predominant. This implies, that dislocations and grain boundaries, which have been observed in transmission electron microscopic (TEM) pictures made by G. Wagner (Universität Leipzig) (Fig. 4.10), do not form shunts. The insufficient insulating properties seem to result from an incorrect stoichiometry of the insulators: QSCV measurements revealed, that there is an excess of metal (positive charges) which lead to defects within the insulator. Nevertheless, the sandwich-structure insulators are promising for the application as gate dielectrics in ZnO-based MISFET.

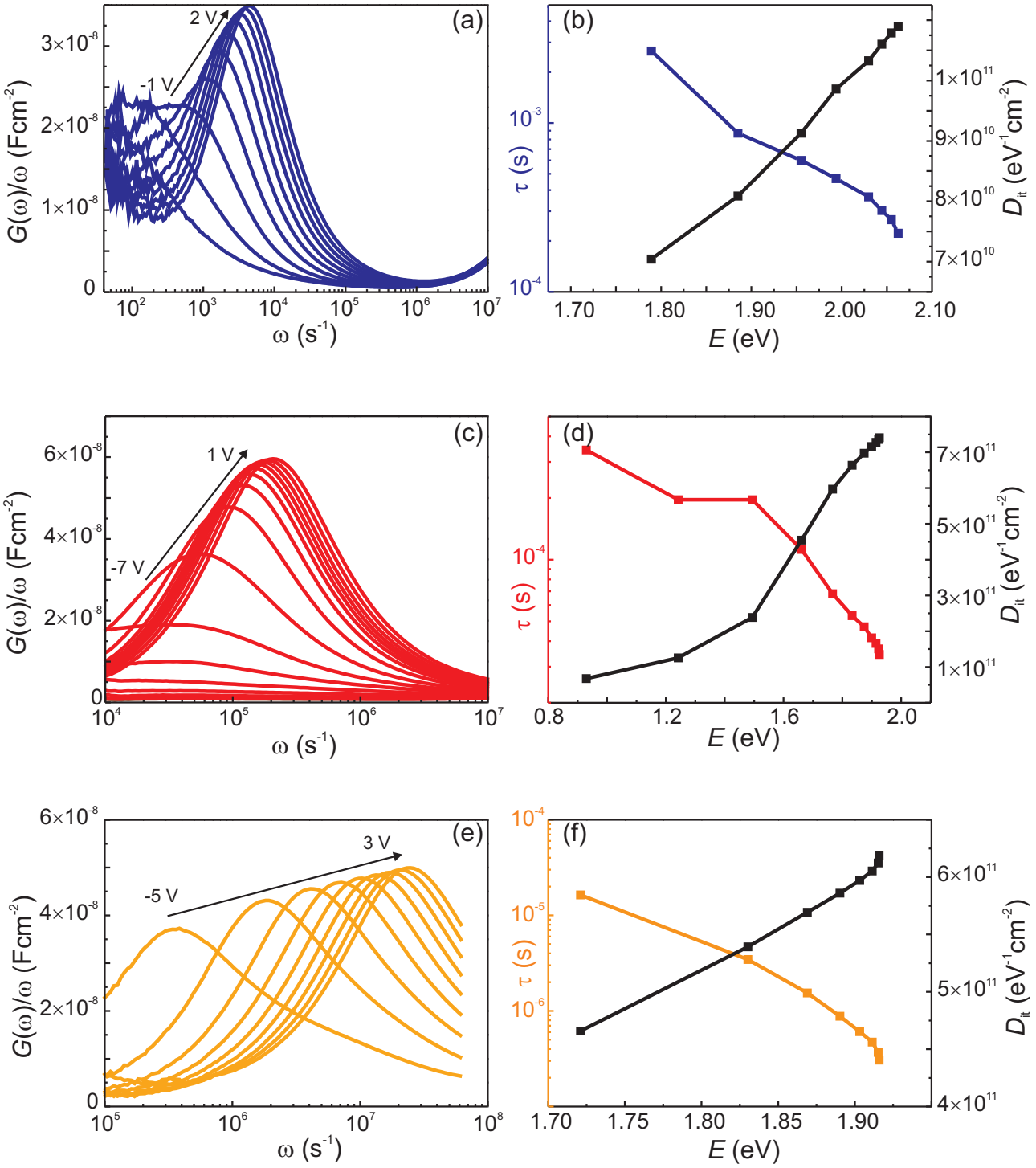


Figure 4.9: Admittance measurements of a-b) a ZrO_2-ZnO-MIS diode, c-d) a HfO_2-ZnO-MIS diode and e-f) a HfO_2-sandwich-structure MIS diode. a,c,e) Voltage-dependent conductance. b,d,f) Interface trap density and time constant.

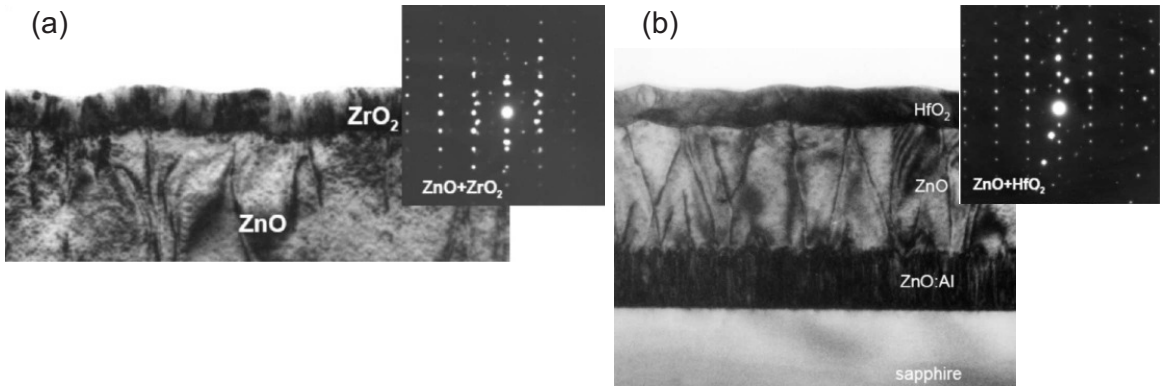


Figure 4.10: Bright-field TEM images of a) ZrO_2 and b) HfO_2 MIS diodes. (Pictures provided by G. Wagner, Universität Leipzig.)

4.3 ZnO-based metal-insulator-semiconductor field-effect transistors

4.3.1 Top-gate ZnO MISFET

Based on the findings in the previous section, top-gate MISFET were fabricated using an Al_2O_3–HfO_2–Al_2O_3 sandwich-structure insulator [Fre10c]. The 50 nm thick ZnO-channel layer was directly grown on the *a*-sapphire substrate. As described in Sec. 3.3, a lift-off technique was used to define source- and drain contacts. The sandwich insulator layer was grown at a substrate temperature of about 500°C (300 W heater power) and an oxygen partial pressure of 0.002 mbar with a total thickness of 90 nm; i.e. the thickness of the HfO_2 was 40 nm and the thickness of each Al_2O_3 layer was 25 nm. Ti/Au (20 nm/30 nm) ohmic contacts were thermally evaporated.

Figure 4.11 depicts the output and transfer characteristics of the sandwich-structure top-gate MISFET. The output characteristic (Fig. 4.11a) shows, that the MISFET is still in the linear regime up to a source-drain voltage of $V_{SD} = 4\,V$. However, for lower gate voltages, and especially for $V_G = -3\,V$, a pinch-off-behavior is clearly visible; but for $V_{SD} > 2\,V$, the source-drain current starts to increase again. Applying larger $V_{SD} > 4\,V$ results in channel breakdown. The pinch-off curvature decreases for increasing V_G, as the depletion layer below the MIS-gate decreases.

The transfer characteristic (Fig. 4.11b) shows a normally-on behavior with a turn-on voltage of $V_T = -6\,V$. The off-current (and with that the gate-leakage current) lies in the range of $10^{-11}\,A$. An on/off-ratio of $I_{on}/I_{off} = 1.5 \times 10^5$ was achieved within a gate-voltage sweep of 7 V. The minimum subthreshold slope was obained to be 300 mV/decade. It can be seen from the transfer characteristic, that I_{SD} reaches a maximum at $V_G \sim +0.4\,V$ before it decreases again. This value can be correlated to the onset of forward conduction of the MIS diodes described in Sec. 4.2. An accumulation of electrons beyond this point is not possible due to the excessive leakage currents.

The channel mobility of this MISFET was calculated using Eqn. 2.63. With an insulator capacitance of $C_i = 6.71 \times 10^{-8}\,Fcm^{-2}$ obtained from QSCV measurement and a channel width/length-ratio of $W/L = 430\,\mu m/60\,\mu m$, the maximum channel mobility is $\mu_{ch} = 1.9\,cm^2/Vs$. This value is about a

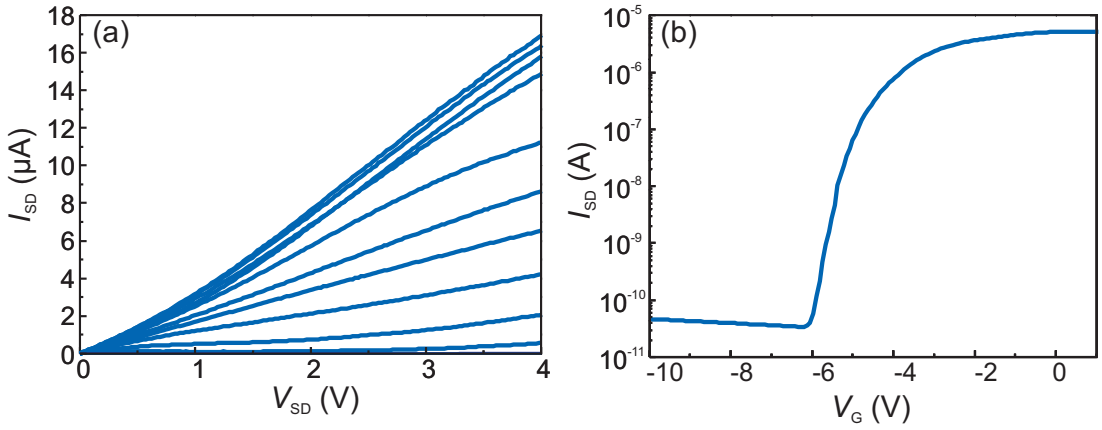


Figure 4.11: a) Output and b) transfer characteristics of a top-gate MISFET with Al_2O_3–HfO_2–Al_2O_3 sandwich-structure insulator.

factor of 10 lower than the measured Hall-effect mobility for the ZnO channel. The reduced channel mobility is due to electron scattering at the ZnO-Al_2O_3 interface. The trapped interface charge density measured by admittance spectroscopy lay in the range of 10^{12} $cm^{-2}eV^{-1}$ (cf. Sec. 4.2).

A comprehensive comparison of MISFET with transparent oxide channels is given in [Gru10]. Only about one third of the reported MISFET are top-gate FET, due to the technological difficulties that occur with the processing of the insulator. Among them, 60% use a pure ZnO channel as within this thesis. Most of them use different growth techniques for the channel and for the insulator. Sputtering techniques are the most common methods for growing gate insulators. Only one report is known, where PLD is used for both the channel and the insulator. Kao *et al.* used a 50 nm thick (Tb, Ce)$MgAl_{11}O_{19}$ gate dielectric for a top-gate ZnO MISFET [Kao05]. They achieved a channel mobility of 5.3 cm^2/Vs but an on/off-ratio of only 10 within a gate voltage range of more than 10 V. The leakage current lay in the range of 10^{-6} A. The reported interface trap density was $\sim 1 \times 10^{10}$ $cm^{-2}eV^{-1}$; two decades lower than for the MISFET in this thesis. Chang *et al.* reported a magnetron sputtered top-gate MISFET using ZnO and a 220 nm thick Al_2O_3–HfO_2–Al_2O_3 sandwich-structure insulator, where the Al_2O_3 layers were each 10 nm thick [Cha08]. Their FET showed normally-off behavior with an on/off-ratio of 10^6 within 10 V V_G-sweep and a channel mobility of $\sim$ 12 cm^2/Vs. They explain the high channel mobility by a charge trapping suppression due to the Al_2O_3 barrier layers. A double layer with 200 nm Al_2O_3 and 100 nm HfO_2 was grown by radio-frequency sputtering in the report of [Hsi06] to fabricate bottom-gate MISFET with ZnO channel. The FET exhibit an on/off-ratio of 10^7 within 14 V V_G-sweep and μ_{ch} = 8.4 cm^2/Vs.

These reports show, that with regard to the channel mobility, the MISFET shown in this thesis still can be improved. However, this can only be done if the metal excess in the PLD-grown insulators is reduced; e.g. using a plasma-assisted PLD like in [Gö06, Gö07b, Gö07a]. With regard to the subthreshold slope, the achieved value of S = 300 mV/decade is comparable to the best values of ZnO MISFET having 210 mV/decade [Kim09b], 250 mV/decade [Kim05a, Sid06] or 400 mV/decade [Kan07b]. Among top-gate MISFET, the presented slope is the highest compared to 500–520 mV/decade [Cha08, Par09].

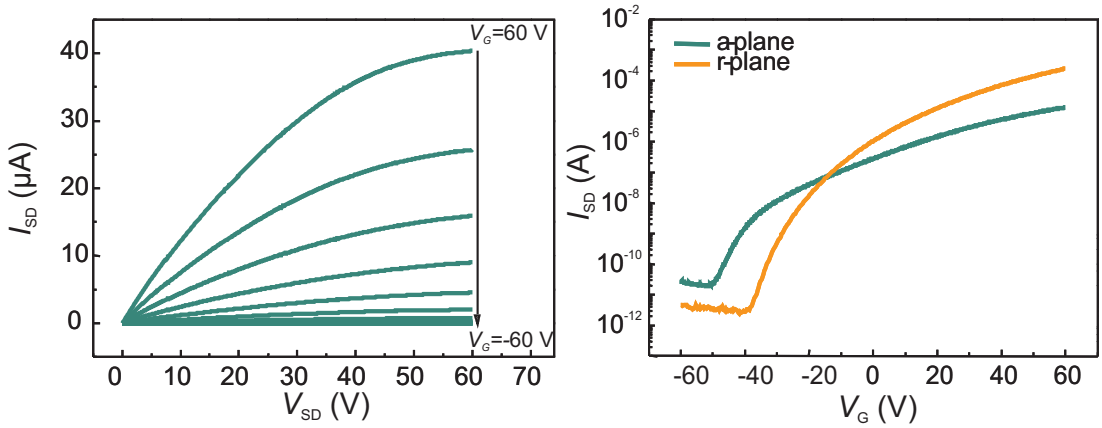


Figure 4.12: a) Output and b) transfer characteristics of bottom-gate MISFET grown on r-plane and a-plane sapphire.

4.3.2 Bottom-gate ZnO MISFET

Bottom-gate ZnO MISFET have been grown by PLD on *a*-plane and *r*-plane sapphire substrate. First, a 140 nm thick bottom-gate contact consisting of Al doped ZnO was grown on the substrate. Then, 860 nm Al_2O_3 was deposited as insulator. Finally, 130 nm undoped ZnO was grown on top of the insulator as channel. The advantages are, that the complete structure can be grown in situ within one PLD step and the photolithographic processing consists of the two steps mesa-etching and source/drain-contacts-metallization. The major disadvantage is the need of the thick insulator. Due to the high-temperature growth of the ZnO channel after deposition of the insulator, diffusion of metals into the insulator and short circuits are more likely in bottom-gate configuration than in top-gate configuration. Note, that a lower-temperature PLD-growth of the ZnO-layer leads to an excess of zinc interstitials [Wen08] resulting in too high conductivity.

Figure 4.12 depicts the output and transfer characteristics of the bottom-gate MISFET on *a*-plane and *r*-plane sapphire substrate. For both MISFET gate voltages of ±60 V are needed to switch between the on- and off-state. Within the applied source-drain voltage of 60 V, the *a*-plane MISFET shows a pinch-off behavior in the output characteristic, whereas the *r*-plane MISFET has a linear behavior comparable to the top-gate MISFET shown in Fig. 4.11b. This is due to the lower free-carier concentration of $6 \times 10^{16}\,\mathrm{cm}^{-3}$ for the *a*-plane MISFET with respect to $2 \times 10^{18}\,\mathrm{cm}^{-3}$ for the *r*-plane MISFET. Obviously, the diffusion of dopants into the channel is more likely for the FET on *r*-plane substrate. The transfer characteristics of the bottom-gate MISFET (Fig. 4.12) show a normally-on behavior with turn-on voltages of $V_T = -50\,\mathrm{V}$ and $V_T = -40\,\mathrm{V}$ for *a*-plane and *r*-plane, respectively. Due to the thick insulator with leakage currents in the range between $10^{-12}\,\mathrm{A}$ and $10^{-11}\,\mathrm{A}$, no forward conduction of the MIS-gate diode occured. With that, the accumulation of electrons in the ZnO channel is possible; i.e. no decrease of I_{SD} could be observed for large positive V_G. The on/off-ratios were 5×10^5 for the *a*-plane MISFET and 6×10^7 for *r*-plane MISFET. Unfortunately, the channel mobilities are very low for the bottom-gate MISFET as compared to the top-gate MISFET. The values were $\mu_{ch} = 0.3\,\mathrm{cm}^2/\mathrm{Vs}$ and $\mu_{ch} = 0.5\,\mathrm{cm}^2/\mathrm{Vs}$ for *a*-plane and *r*-plane, respectively. Similar channel mobilities were also observed for a bottom-gate MISFET using an equally grown ZnO channel and a ferroelectric $BaTiO_3$-insulator on $SrTiO_3$ substrate [Bra09a].

5 ZnO-based metal-semiconductor field-effect transistors

Based on highly rectifying Schottky diodes as gate contacts, MESFET were fabricated as described in chapter 3. As will be shown in the following sections, MESFET exhibit some distinct advantages compared to MISFET. Figure 5.1 depicts the transfer characteristics of the best top-gate MISFET as shown in Sec. 4.3 and a MESFET with gate width-to-length-ratio of 21.5 (cf. Sec. 5.1.1). The MESFET has a much higher on/off-ratio, higher mobility and steeper subthreshold slope within a lower gate-voltage sweep. Therefore, ZnO-MESFET are further investigated regarding design possibilities, reliability and degradation effects. The results will later be used within integrated inverter structures (Cha. 6) and fully transparent devices (Cha. 7).

The pre-characterization of each MESFET sample was performed using room-temperature Hall-effect measurements done by Matthias Brandt, Robert Heinhold or Thomas Lüder at Univerität Leipzig in order to obtain the channel layer's free carrier concentration and electron mobility, as well as spectroscopic ellipsometry measured by Chris Sturm, Helena Hilmer or Rüdiger Schmidt-Grund at Universität Leipzig, to obtain the thickness of the ZnO thin film.

5.1 Sapphire substrate

Most of the results in this thesis were obtained for *a*-plane sapphire substrates. It is used as standard substrate allowing epitaxial growth of high-quality ZnO thin films. XRD revealed that the ZnO is in the *c*-oriented single crystalline state, textured with small angle grain boundaries [Wen07a]. For a 1 µm thick ZnO layer, the X-ray rocking curve width is typically 370 arcsec [Wen07c], the channel layer used for the MESFET, having thicknesses in the range of 20–30 nm exhibit much larger broadening. In such close vicinity to the substrate, the crystal quality is affected by dislocations.

5.1.1 ZnO-MESFET design

Gate material

For successful operation of MESFET devices, a gate metal with a high Schottky barrier is needed. Therefore, the influence of different Schottky-gate metals on the Schottky-, output and transfer characteristics of ZnO-based MESFET has been systematically investigated. Reactively sputtered Ag, Pt, Pd and Au gates (Tab. 3.2) were used for this purpose [Fre09a]. It has been shown by A. Lajn *et al.* [Laj09], that the effective Schottky barrier height increases for reactively sputtered, partially oxidized Schottky metals on ZnO thin films. Figure 5.2 depicts room-temperature IV measurements of such Schottky contacts measured at the final MESFET structure between source and gate contact in

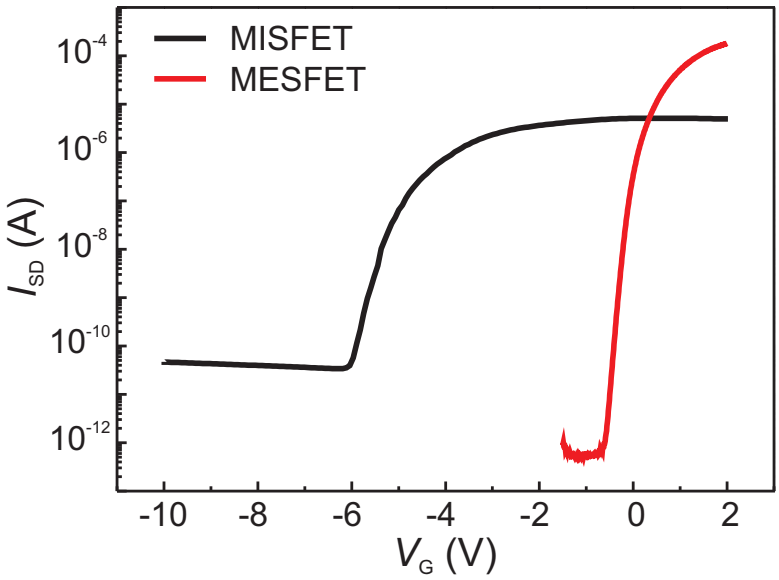


Figure 5.1: Transfer characteristics of the best top-gate MISFET (cf. Fig. 4.11b) and MESFET (cf. Fig. 5.7b, $W/L = 21.5$).

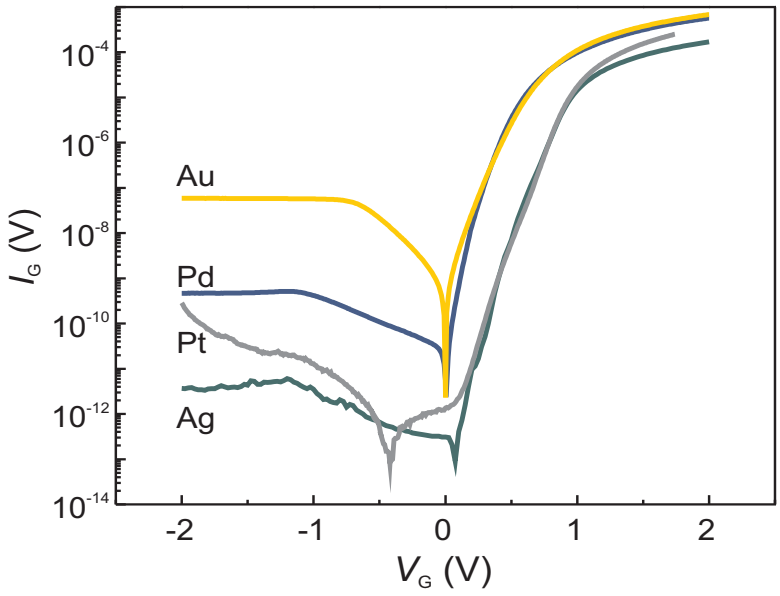


Figure 5.2: Room-temperature IV Schottky-gate characteristics of MESFET with Ag, Pt, Pd, and Au.

front-to-front configuration. The characteristics were analyzed using the thermionic emission model as described in Sec. 2.1.3 including parameters for the serial and parallel resistances and the ideality factor (Eqn. 3.2). The results are summarized in Tab. 5.1. Values for the parallel resistance are omitted (without an effect on the other values) due to the non-ideal Schottky-like behavior in reverse direction. The characteristics for Ag, Pd and Au show a pinch-off, which is due to the low channel thickness of the MESFET. The increase of the reverse current can be attributed to inhomogeneous barrier heights [Wen06].

Table 5.1: Properties of the gate diodes of Ag, Pt, Pd and Au MESFET at room-temperature.

Gate metal	rect.-ratio at ±2 V	R_S (kΩ)	Φ_B (V)	η
Ag	5×10^7	5.8	0.95	1.7
Pt	3×10^6	2.4	0.90	2.04
Pd	1.1×10^6	2.0	0.79	1.53
Au	1.2×10^4	1.6	0.69	2.37

As expected, the Schottky barrier heights are higher than typically observed barrier heights on ZnO [Oez05]. For Au Schottky contacts on ZnO, it is similar to the highest barrier of 0.71 V observed by Mead *et al.* [Mea65]. The barrier height of Pt is in good agreement with Kim *et al.* who reported values between 0.89 V and 0.93 V on hydrogen peroxide treated ZnO [Kim05b]. Allen *et al.* reported Schottky contacts on hydrothermally grown ZnO single crystalls with reactively sputtered Ag [All07, All09]. They observed high Schottky barriers and ideality factors close to unity. The formation of an oxide was also observed for the here presented Ag, Pt and Pd contacts [Laj09].

The impact of the various gate metals on the performance of the MESFET at room-temperature is depicted in Fig. 5.3. The characteristics were obtained from samples that were grown under nominally identical growth conditions. An overview of the measured MESFET properties is given in Tab. 5.2.

The MESFET were operated in a source-drain voltage range between 0 and 2 V and show clear saturation and pinch-off behavior. Change of the gate voltage between +1 V and, depending on the turn-on voltage, up to −2 V leads to a change of the channel conductance and the FET can be switched on and off. As one can see, forward gate voltage values near or higher than the barrier height of the gate Schottky contact cause flatband condition and therefore higher gate leakage currents. This results in a shift of the individual output curve as clearly observed for the Pd- and Au-gate MESFET reflecting their lower Schottky barriers (Fig. 5.3d and e). All MESFET are normally-on; i.e. the channel is conductive at zero gate voltage. In the on state, they reach source-drain currents in the range of several 10 micro amperes. The higher source-drain current for the Pd- and Au-gate MESFET is caused by the lower series restistance of the ZnO channel and the higher conductivity due to higher electron mobility. The comparison of transfer characteristics at $V_{SD} = 2$ V (Fig. 5.3a) shows a strong field-effect for all MESFET. The highest on/off-ratio exceeds eight orders of magnitude for the Ag-MESFET with a low off-current in the sub-picoampere range and a turn-on voltage of $V_T = -1.4$ V. The Pt-, Pd-, and Au-MESFETs are more affected by leakage currents, which increase the off current. Nevertheless, for Pt, the on/off-ratio still exceeds six decades, whereas it is only five decades for Pd and three decades for Au. The turn-on voltages of the devices with Pt, Pd, and Au are $V_T = -1.1$ V, $V_T = -1.2$ V, and $V_T = -0.7$ V, respectively, reflecting the higher off-currents. The differences in the characteristics can be explained by different channel thicknesses and the different Schottky contact's barrier heights and built-in potentials resulting in a different depletion layer depth (Eqn. 2.7).

The channel mobilities of the MESFET were calculated using the maximum forward transconductance in the saturation regime and Eqn. 2.54 as described in Sec. 2.3.1. The values are summarized in Tab. 5.2. They are about a factor of 10 higher than usually observed channel mobilities in ZnO-based MISFET that were described in Sec. 4.3. For Ag, Pt and Pd, μ_{ch} is in good agreement with the measured Hall-effect mobility, which confirms the expectation from the MESFET theory that the

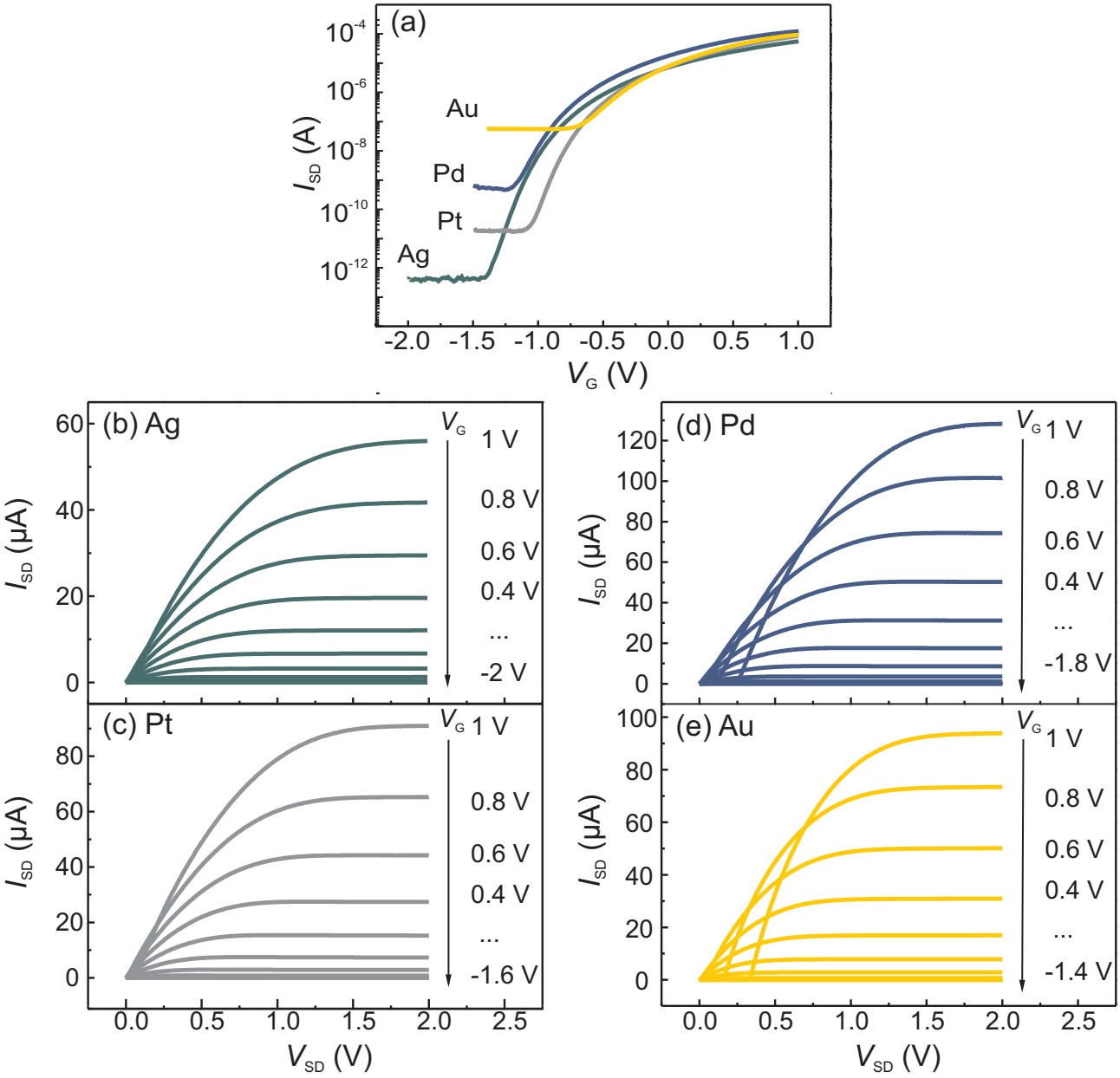


Figure 5.3: Comparison of various Schottky gate materials at room-temperature. a) Transfer characteristics. b-e) Output characteristics of MESFET with b) Ag, c) Pt, d) Pd and e) Au.

Table 5.2: Overview of the measured MESFET properties.

Gate metal	d (nm)	$N_D - N_A$ (10^{18} cm^{-3})	μ_{Hall} (cm^2/Vs)	μ_{ch} (cm^2/Vs)	on/off-ratio	S_{min} (mV/decade)
Ag	20	2.8	9.3	11.3	1.2×10^8	81
Pt	26	2.4	12.1	11.4	4.5×10^6	83
Pd	26	2.4	12.1	12.8	2.6×10^5	156
Au	20	1.5	43.9	23.9	1.6×10^3	282

channel mobility equals the Hall-effect mobility of the respective semiconductor [Zeg04]. However, this statement is not generally valid. The channel mobility can be over- or underestimated under the presence of parasitic effects, e.g. excessive gate currents. This is the case for the Au-MESFET. Its μ_{ch} is significantly lower than μ_{Hall}. This is caused by the higher negative gate leakage current, which is responsible for the shift of the output characteristic (Fig. 5.3e). It lowers the channel's transconductance and thus the mobility is underestimated. In general, the mobilities in this thesis are lower than typically observed mobilities for ZnO PLD thin films [Wen07b]. This may be due to the larger influence of a low-mobility degenerate layer at the ZnO/sapphire-interface, the higher defect density and smaller grains in the thin films [Ort80].

As can be seen in Fig. 5.3a, in the vicinity of the MESFET turn-on voltage, the slope S of the transfer characteristics is found to be exponentially dependent on the gate voltage. For low-power applications, this slope is important and affects the switching speed of integrated circuits; i.e. S has to be as small as possible. The obtained minimal values are given in Tab. 5.2. The values for Ag and Pt are already close to the theoretical minimum for FET operating at room temperature

$$S_{\min} = \ln(10)(k_B T/q) \approx 60\,\mathrm{mV/decade}\,. \tag{5.1}$$

This model is based on electron diffusion through the depletion region [Lia91] and is valid for MESFET as well as depletion-mode MISFET. For the real slope, in both cases, an ideality factor N_S has to be added to Eqn. 5.1, which considers the leakage currents for MESFET [Jit09] or capacitances for MISFET [Sze81]. Close to the turn-on voltage, the channel is almost closed and the pinch-off point is moving towards the source electrode. The electron injection into the channel is then limited by the potential barrier of the depletion region under the gate, which leads to the exponential dependence of I_{SD} on V_G. The injected electrons diffuse through the depletion region towards the drain electrode, where they are collected. For higher V_G, the channel is more open and the electrons drift through the conductive path below the depletion region; S is rapidly increasing. For positive V_G, the fraction of gate leakage current in I_{SD} increases and affects the transfer curve. Thus, the smaller slopes for Pd and Au are explainable with the lower Schottky barrier heights of these contacts and consequently with the higher gate leakage current. Nevertheless, the slopes obtained for the MESFET are lower than the slopes of the MISFET presented in Sec. 4.3 and among the lowest values for oxide FET in general. Wang *et al.* reported a MISFET based on an In_2O_3 channel with organic pentacene insulator with a slope of $S = 90\,\mathrm{mV/decade}$. Several more reports exist, where slopes between 108 mV/decade and 180 mV/decade where achieved, using amorphous gallium indium tin oxide as semiconductor channel [Nom08, Sat09, Na08a, Cho09].

Based on the previous results, MESFET with Ag-gates were chosen to be the standard for the forthcoming investigations. They exhibit the lowest gate-leakage currents as well as the steepest slopes. However, for the application of ZnO MESFET as e.g. driving transistor for active-matrix organic-light-emitting-diode (AMOLED) displays, a higher on-current in the range of milliamperes is necessary [Gö09]. From the proportionality of the source-drain current in Eqn. 2.52 with Eqn. 2.48:

$$I_{SD} \propto e\mu_{ch}(N_D - N_A)d\frac{W}{L}\,, \tag{5.2}$$

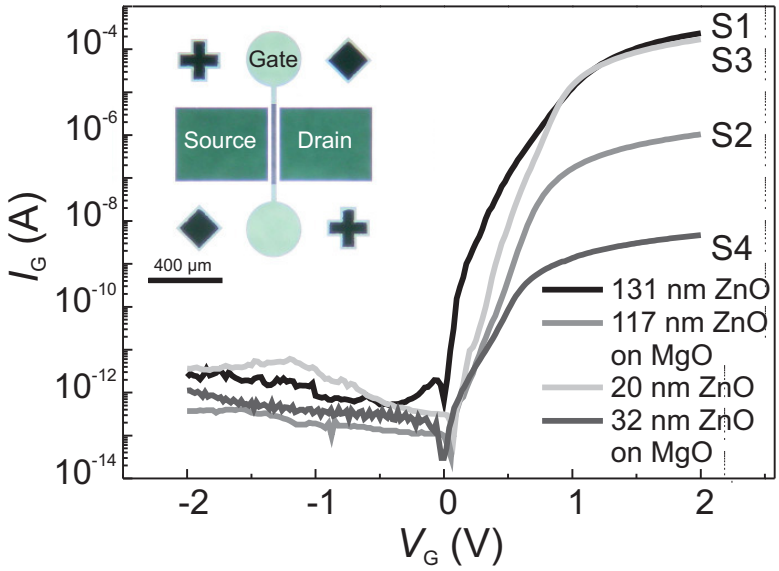


Figure 5.4: Room-temperature IV characteristics of Ag-Schottky gates on MESFET with different channel layer configurations. Inset: Optical microscopic image of a ZnO MESFET.

the optimization of MESFET can be achieved by increasing a) the channel thickness d, b) the net doping concentration $N_D - N_A$, c) the gate's width-to-length ratio W/L or d) the channel-mobility μ_{ch} under perpetuation of the high dynamic of the MESFET, i.e. equal off-currents, turn-on voltages, saturation- and pinch-off-behavior. This is the subject of the following paragraphs.

Net doping concentration and channel thickness

The influence of the net doping concentration and channel thickness on the performance of MESFET on sapphire substrate have been investigated [Fre08]. Since the free carrier concentration in the nominally undoped ZnO is determined by the diffusion of Al from the sapphire substrate during PLD growth, a MgO thin film was used as insulating buffer layer before growth of the ZnO channel. The MgO buffer layer has been in situ annealed for 20 minutes at 5×10^{-5} mbar oxygen partial pressure and 600°C. Four layer configurations were investigated: two samples, denoted as S1 and S2, consist of thick (S1: 131 nm, S2: 117 nm) nominally undoped ZnO layers directly grown on sapphire (S1) and on the 30 nm thick MgO-buffer (S2); the second two samples, S3 and S4, are MESFET with thin (S3: 20 nm, S4: 32 nm) undoped ZnO layers on sapphire (S3) and on MgO-buffer (S4). The measured properties of the MESFET are given in Tab. 5.4. Note, that sample S3 is identical to the Ag-MESFET sample, which has been previously investigated (Tabs. 5.1 and 5.2).

IV characteristics of the Ag gate Schottky contacts are depicted in Fig. 5.4 and summarized in Tab. 5.3. They show an excellent rectification behavior with leakage currents in the range of picoamperes. High Schottky barrier heights of 0.95 V are reproducibly achieved. The forward current is limited by the series resistance R_S, which is drastically higher for the samples with MgO-buffer (S2 and S4).

A comparison of transfer characteristics obtained at $V_{SD} = 4$ V is shown in Fig. 5.5. An overview of the measured MESFET properties is given in Tab. 5.4. The net doping concentration for the samples

Table 5.3: Properties of the gate diodes of Ag_xO MESFET with different channel layer configurations.

Sample	rect.-ratio at ±2 V	R_S (kΩ)	Φ_B (V)	η
S1	6×10^7	5	0.95	2.0
S2	2×10^6	10^3	0.95	1.6
S3	5×10^7	5.8	0.95	1.7
S4	3×10^3	2×10^5	0.95	3.0

Table 5.4: Overview of the measured MESFET properties.

Sample	Layers	d (nm)	$N_D - N_A$ (cm^{-3})	μ_{Hall} (cm^2/Vs)	μ_{ch} (cm^2/Vs)	on/off-ratio	S_{min} (mV/decade)
S1	ZnO	131	5×10^{17}	15.4	19.1	–	–
S2	ZnO+MgO	117	1.5×10^{14}	29.4	27.4	4×10^4	432
S3	ZnO	20	2.8×10^{18}	9.3	11.3	1.2×10^8	81
S4	ZnO+MgO	32	–	9.7	–	–	–

with MgO buffer is reduced by four to five orders of magnitude compared to the samples directly grown on sapphire. Thus, it is necessary to increase the channel thickness in order to ensure that the depletion region can be modulated within sufficient gate voltages. Note, that the forward voltage is limited to about 1 V, which coincides with the built-in voltage of the Schottky contact. Then, the depletion region is reduced to zero and the channel is fully conductive. An accumulation mode is not possible for MESFET since larger forward gate voltages only increase the leakage current over the Schottky gate. Only the samples S2 and S3 show a strong field effect. The current for S3 can be tuned over 8 decades in a gate-voltage range of only 2.5 V, whereas the on/off-ratio of S2 is only 4×10^4. Both samples exhibit normally-on behavior having equal turn-on voltages of $V_T = -1.5$ V. S1 can be denoted as "static-on" showing no significant field effect in the applied voltage range. Its output characteristic showed linear behavior, i.e. no pinch-off and saturation. It can be concluded, that the channel thickness d of S1 is too large for the obtained doping concentration. On the other hand, S4 can be denoted as "static-off". With a free carrier concentration determined from Hall-effect measurements below 10^{13} cm^{-3}, it is insulating and no modulation of I_{SD} was observed. However, for S1, S2 and S3, μ_{ch} was calculated from g_{max} using Eqn. 2.54. According to Eqn. 2.53, for S1, g_{max} was obtained from the drain transconductance for $V_{SD} \to 0$, since S1 did not show saturation, whereas for S2 and S3, g_{max} was calculated using the forward transconductance of the transfer characteristic in the saturation regime. The channel mobilities are again in good agreement with the Hall-effect mobilities of the unstructured channel layers (cf. Tab. 5.4). Due to the insulating properties of S4, a determination of the net doping concentration via capacitance measurement and the calculation of μ_{ch} was not possible. It is noticeable, that both of the thicker channels have higher mobilities than the two thinner channels. This can be understood, since the dislocation density is larger close to the Al_2O_3-ZnO-interface.

All three variations from the standard MESFET sample S3 have lead to inferior results. The larger thickness of the nominally undoped ZnO channel on sapphire (S1) was not successful since the depletion layer extended such that the channel is closed within the investigated voltage range. The thicker

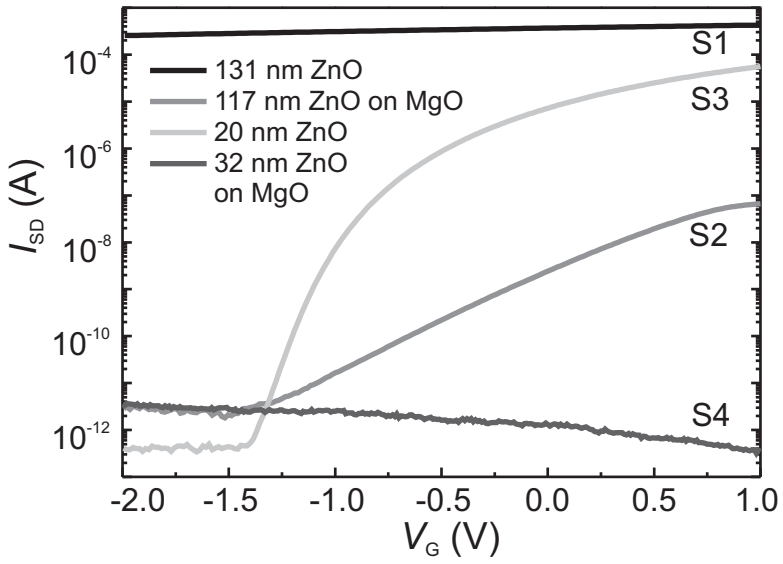


Figure 5.5: Transfer characteristics of Ag-gate MESFET with various channel layer configurations.

channel on MgO buffer (S2) showed a field-effect. However, the on/off-ratio was smaller and the slope was more gentle than for S3. Finally, the thin channel on the MgO buffer (S4) did showed a negligible conduction of the channel. The MgO-buffer layer worked well as diffusion barrier for Al from the sapphire. The channel's net doping concentration was drastically reduced making an intentional doping possible. Therefore, a series of samples was grown consisting of a 50 nm thick Al-doped ZnO channel layer on MgO buffer, where the Al-content of the used PLD-target was 0.001 wt-%, 0.01 wt-%, 0.1 wt-%, and 1 wt-%, respectively. The different Al-contents lead to monotonically increasing net doping concentrations between 1.9×10^{18} cm^{-3} for 0.001 wt-% Al and 7.5×10^{18} cm^{-3} for 0.1 wt-% Al and then decreases to 6.2×10^{18} cm^{-3} for 1 wt-% Al. Even the smallest Al-content in the PLD target results in a rather high net doping concentration; i.e. it is close to the critical Mott concentration of $n_c = 8.3 \times 10^{18}$ cm^{-3} for ZnO [Bra09b]. Although, all Al-doped MESFET did show a field-effect, their performance was rather poor. Figure 5.6 shows the dependence of the on-current, the on/off-ratio and the channel mobility of the processed MESFET. Unexpectedly, the on-current decreases with increasing Al content. This is due to the lower incorporation of Al as donor into the ZnO host lattice. However, XRD measurements did not show any parasitic insulating phases like zinc aluminates. Probably, the Al is accumulated at grain boundaries, where it is not electrically active. Due to the high doping concentrations and increasing probability of scattering on charged impurities, μ_{ch} is decreasing. For Al contents between 0.001 wt-% and 0.1 wt-%, the off-currents were in the range of several ten nanoamperes and the breakdown probability of the Schottky-gate diode was higher. For the MESFET with 1 wt-% Al content, the off-current was again in the range of ten picoamperes, comparable to the undoped ZnO-channel and the on/off-ratio was 10^6. Hence, even lower target concentrations are needed, e.g. by means of an alternating-target PLD.

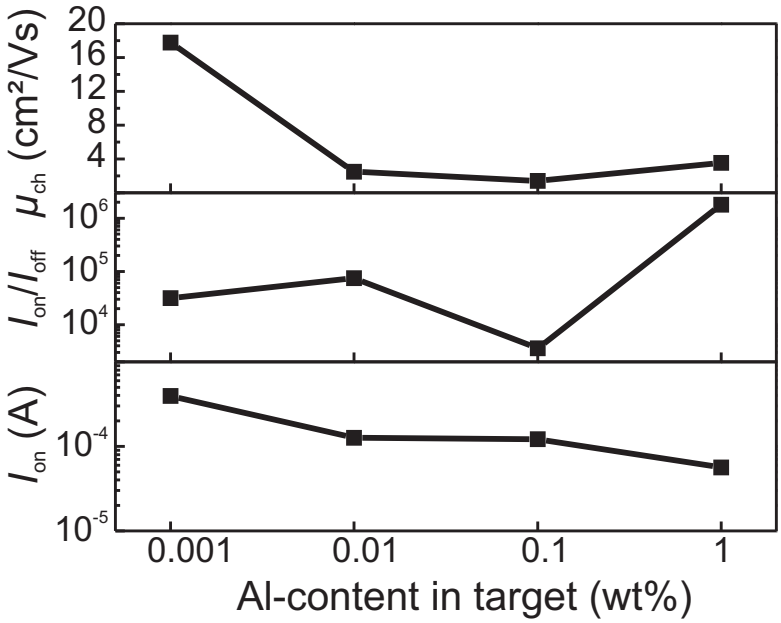


Figure 5.6: Channel mobility, on/off-ratio and on-current of MESFET with various Al-doped ZnO channels on MgO buffer.

Gate width-to-length-ratio

The on/off-ratio is ostensibly determined by leakage currents over the gate and also through the MgO buffer. The previous investigations suggest that for the used PLD-growth method of the ZnO channel on sapphire, the parameters for the standard sample S3 (channel thickness in the range of 30 nm, net doping concentration from 10^{17} cm^{-3} to 10^{18} cm^{-3}, no buffer layer) were most appropriate for best MESFET performance. In order to increase the source-drain current in the on-state of the MESFET, the W/L-ratio is varied. MESFET with interdigitated source-drain contacts and meander-shaped gate contacts between them have been designed (see inset of Fig. 5.7a). The gate length was kept constant at 10 μm; whereas the width was varied such that the W/L-ratio was in the range between the standard value $W/L = 10.75$ and $W/L = 700$. Figure 5.7a shows transfer characteristics of various ZnO MESFET with different W/L-ratios. A maximum on-current of 15 mA and an on/off-ratio of 5×10^8 was achieved with $W/L = 700$. Such a MESFET is suitable to provide an adequate current for the operation of a pixel of an active-matrix OLED display [Gö09]. It can be seen from Fig. 5.7b, that the transconductance, obtained from the forward source-drain current, scales with the W/L-ratio as expected from Eqn. 5.2, whereas the channel mobility stays constant at a mean value of 5.8 cm^2/Vs up to $W/L = 67.5$. For higher W/L-ratios, μ_{ch} is underestimated compared to the value for standard geometry due to the increasing influence of gate currents.

Channel mobility

The channel mobility can be increased by improving the crystal quality of the ZnO channel. This can be done by growing the ZnO thin film homoepitaxial on ZnO substrates as shown in [Wen07c]. Two MESFET samples have been fabricated. For one sample, a standard ZnO-channel was directly grown

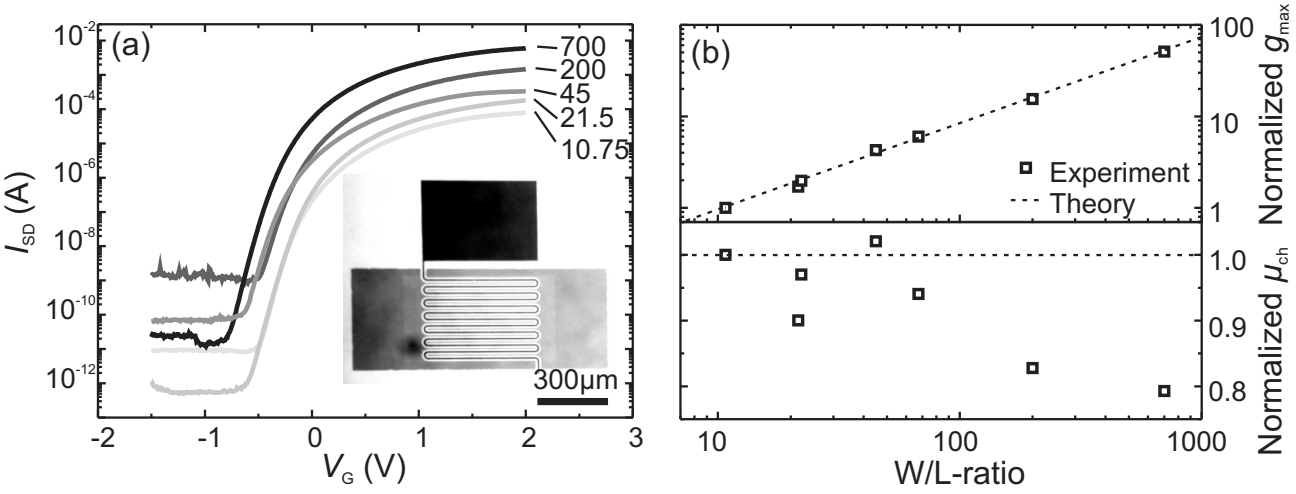


Figure 5.7: a) Transfer characteristics of ZnO-MESFET with different W/L-ratios from 10.75 to 700. Inset: Optical image of the MESFET with $W/L = 700$ and interdigitated contact geometry. b) W/L-ratio scaling behavior of the MESFET. The transconductance and mobility is normalized with respect to the standard geometry $W/L = 10.75$.

Table 5.5: Properties of the gate diodes of homoepitaxial MESFET with and without MgZnO buffer layer.

Sample	rect.-ratio at ±1 V	R_S (kΩ)	Φ_B (V)	η
with buffer	8.4×10^4	2.8×10^3	0.94	1.75
w/o buffer	2.3×10^4	1.78	0.85	1.93

on the ZnO substrate. For the other sample, a MgZnO buffer layer was grown between the substrate and the ZnO-channel. Figure 5.8 depicts atomic force microsopic (AFM) images of the ZnO surface with and without buffer layer. On the one hand, the MgZnO buffer layer reduces the surface roughness (Fig. 5.8a). But on the other hand, the sample without buffer layer showed 2-dimensional growth of the ZnO channel layer with $c/2$-steps. Both channels have less grain boundaries as compared to heteroepitaxial growth on sapphire. The dislocation density was reduced to a range of 10^8 cm^{-2}.

MESFET have been fabricated on these films and electrical measurements have been performed [Fre10c]. IV measurements of the Schottky gate-contacts and their results are given in Fig. 5.9 and Tab. 5.5, respectively. It can be seen, that the ZnO channel without buffer layer is more conductive than the one with MgZnO buffer layer indicating, that the MgZnO is an effective diffusion barrier for impurities coming from the substrate. However, the sample without buffer layer shows a much higher reverse current due to a parallel resistance, which comes from the not sufficiently insulating ZnO substrate. This will cause cross-talk between individual MEFET. Figure 5.10 shows the output characteristic of the MESFET with buffer layer. A pinch-off or saturation behavior was not distinctive. The applied gate-voltage sweep from +1 V to −3 V only results in a small modulation of the source-drain current. For the sample without buffer layer, no field-effect could be observed. Nevertheless, μ_{ch} has been determined for both samples from the drain transconductance in the linear drift regime. The results are summarized in Tab. 5.6. As expected from the AFM pictures, the sample without buffer layer has the higher crystal quality and thus exhibits a higher channel and Hall-effect

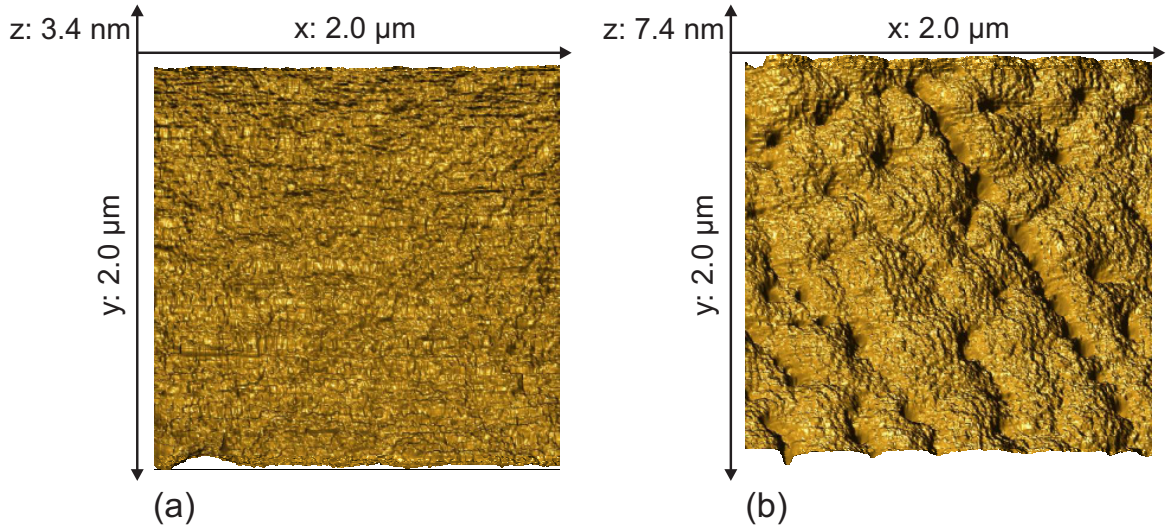


Figure 5.8: AFM pictures comparing the surface of homoepitaxially grown ZnO thin film channels. a) with MgZnO buffer layer and b) without buffer layer. (Data measured by M. Brandt, Universität Leipzig.)

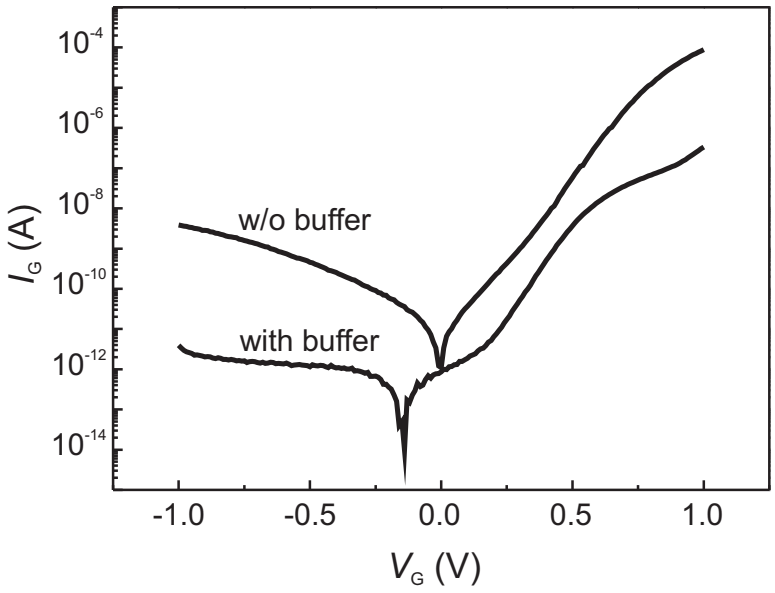


Figure 5.9: IV Schottky characteristics of homoepitaxial MESFET with and without MgZnO buffer layer.

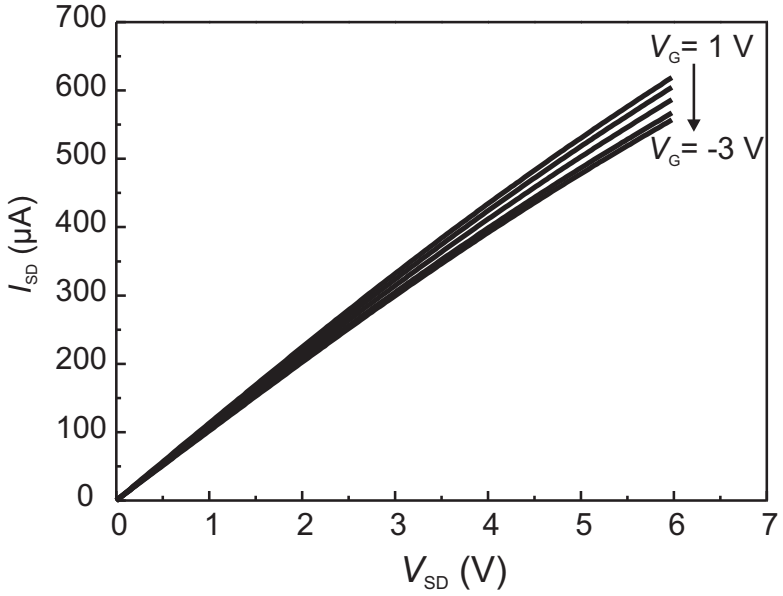


Figure 5.10: Output characteristic of the homoepitaxial MESFET with MgZnO buffer layer.

Table 5.6: Overview of the measured properties for homoepitaxial MESFET.

Sample	d (nm)	$N_D - N_A$ (cm^{-3})	μ_{Hall} (cm^2/Vs)	μ_{ch} (cm^2/Vs)
with buffer	~50	6×10^{17}	90	18
w/o buffer	~50	3×10^{18}	150	50

mobility. The value of μ_{ch} = 50 cm^2/Vs is the highest obtained for MESFET in this thesis. However, temperature-dependent Hall-effect measurements on this sample revealed a mobility of 150 cm^2/Vs at room-temperature. The Hall mobility (Fig. 5.11) could be best fitted using a model without grain boundary scattering. The main scattering mechanism is ionized impurity scattering. For the sample with buffer layer, the low mobilities are probably due to higher compensation and additional scattering at the ZnO/MgZnO interface. The discrepancy between the mobilities implies that the semi-insulating ZnO substrate with a doping concentration in the range of 10^{14} cm^{-3} still carries too much current which results in insufficient saturation and underestimated channel mobilities.

A further increase of the channel mobility could be achieved using a two-dimensional electron gas (2DEG) in a MgZnO/ZnO/MgZnO quantum well (QW) heterostructure [Fre10c]. The 5 nm thick ZnO-QW was embedded in 100 nm thick Ga-doped MgZnO barrier layers. As can be seen in Fig. 5.12a, the charging of the QW has been observed by current-voltage measurements at a voltage of around 0.5 V. At the same voltage, the forward transconductance of the MESFET (Fig. 5.12b) reveals a sharp increase in the transfer measurement. This implies electron transport through the QW, where the channel mobility is higher than in the surrounding barrier. However, the source-drain current is rather small due to low carrier injection through the MgZnO:Ga barrier. The channel mobility could not be determined due to the insufficient doping concentration within the barrier.

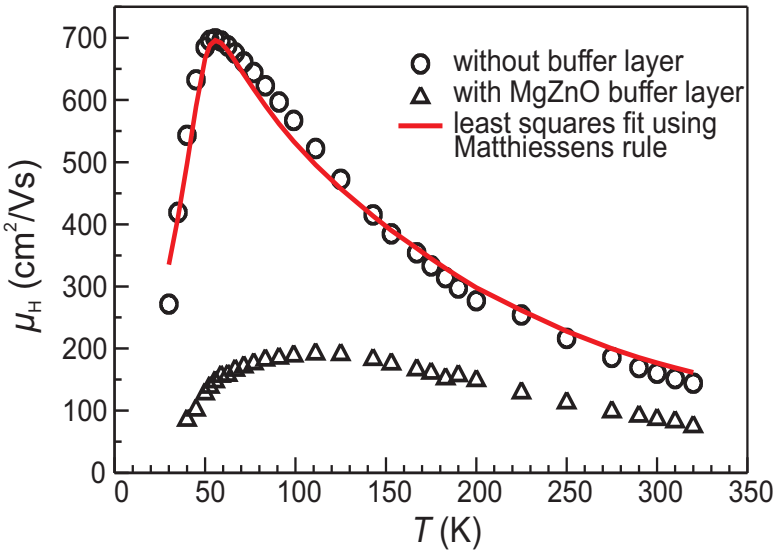


Figure 5.11: Temperature-dependent Hall-effect measurements of the homoepitaxial MESFET channel layers. (Data measured by M. Brandt, Universität Leipzig.)

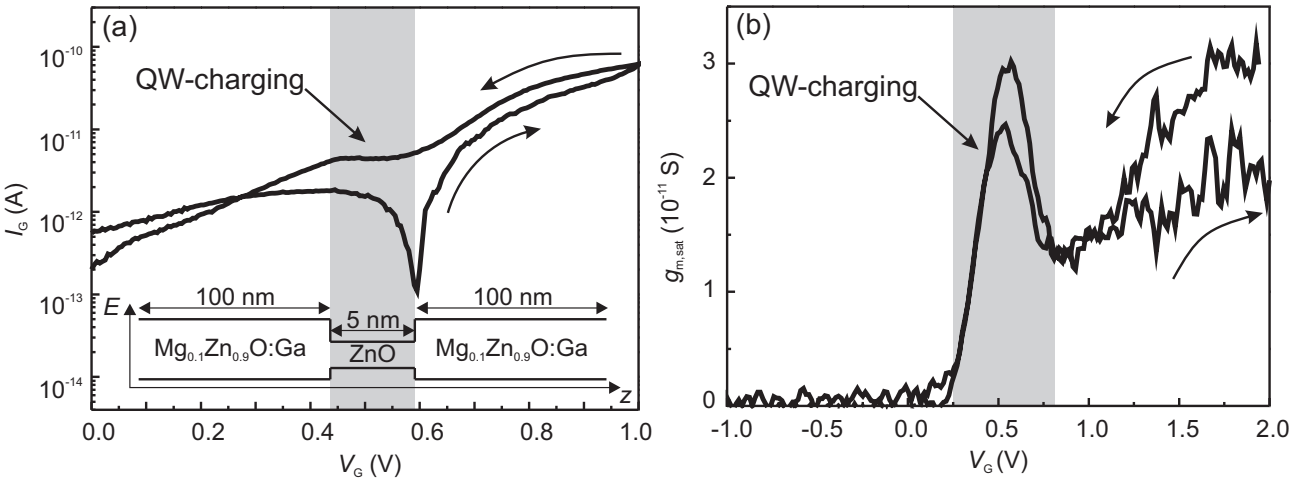


Figure 5.12: a) IV-measurement of the gate Schottky diode and b) forward transconductance in the saturation regime of a MESFET with MgZnO/ZnO/MgZnO quantum-well (QW) channel. Inset: Scheme of the used QW-structure.

The use of highly sophisticated channel structures for the realization of high electron mobility transistors (HEMT) on the basis of ZnO MESFET technology will only be reasonable for applications in transparent electronics as part of circuits that operate in the GHz range. In the meantime, it has been shown (cf. Sec. 5.2) [Fre09c] that the ZnO-MESFET technology can be transferred to near-term industrially more significant and cheaper glass substrates for the production of transparent low-cost electronics in display applications.

5.1.2 Reliability and degradation

Elevated temperatures

In order to investigate degradation effects, Ag-, Pt-, Pd-, and Au-MESFET were tested at elevated temperatures between 25°C and 150°C under ambient air atmosphere. For that, the Waferprober's chuck was heated to constant elevated temperatures by means of a *Huber* unichiller and transfer as well as Schottky characteristics of the MESFET were measured for each temperature step [Fre09a].

Considering the ideality factor η and barrier height Φ_B of the Schotty gate contacts, an annealing effect was observed for Ag, Pt, and Au (Fig. 5.13a, b). The ideality factor is decreasing up to a temperature of 100°C (for Au until 125°C), whereas the barrier height is increasing up to maximum values of 1.14 V for Ag, 1.07 V for Pt, and 0.97 V for Au. The values for Pd, however, are almost constant at $\eta = 1.5$ and $\Phi_B = 0.82$ V in the temperature range between 25°C and 100°C. It applies to all MESFET that a significant increase of the temperature above 100°C leads to irreversible damage at the Schotty contacts (cf. [Wen10b]).

As can be seen in Fig. 5.14, degradation of the Schottky contacts leads to an increasing off-current for the MESFET due to higher gate leakage currents. The off-current is monotonically increasing for the Pd MESFET (Fig. 5.14c), whereas it stays constant for Pt up to 75°C before it increases (Fig. 5.14b). For Ag, a significant decrease of the off-current is observed for temperatures between 25°C and 75°C (Fig. 5.14a). Not before 100°C, it starts to increase drastically with increasing temperature. This annealing effect is more distinctive for Au, as its Schottky-contact properties are improving up to 125°C. Thus, the Pd-, Pt-, Ag-, and Au-MESFET are stable at least for temperatures up to 50°C, 75°C, 100°C, and 125°C, respectively. Within this temperature range, a shift of the characteristics (and the turn-on voltage) towards smaller negative voltages is observed. For Ag, Pt and Au, it is approximately $\Delta V_T = 200$ mV, $\Delta V_T = 250$ mV, and $\Delta V_T = 440$ mV, respectively. The increasing Schottky barrier height leads to a higher built-in voltage and therefore to a larger depletion layer width. Lower gate voltages are necessary to deplete the channels. Since Φ_B stays constant for the Pd-MESFET, this effect is not distinctive for this device.

In the on-state of the MESFET, the transconductance and with that the channel mobility (Eqn. 2.54) is monotonically decreasing with increasing temperatures due to the increasing scattering rate at lattice vibrations and gate-leakage effects. Here, no advancement due to annealing can be observed (Fig. 5.13c). However, there are small differences between the used Schottky-gate metals. For Pt- and Pd-gate devices, the negative slope of the channel mobility increases at 75°C. Then, for higher temperatures, it is steeper for the Pd-sample indicating a faster degradation. For Ag, the slope does not increase until 100°C resulting in a similar slope as for the Pt-sample. The channel mobility for Au decreases more drastically as compared to the other metals, which is probably due to the a priori

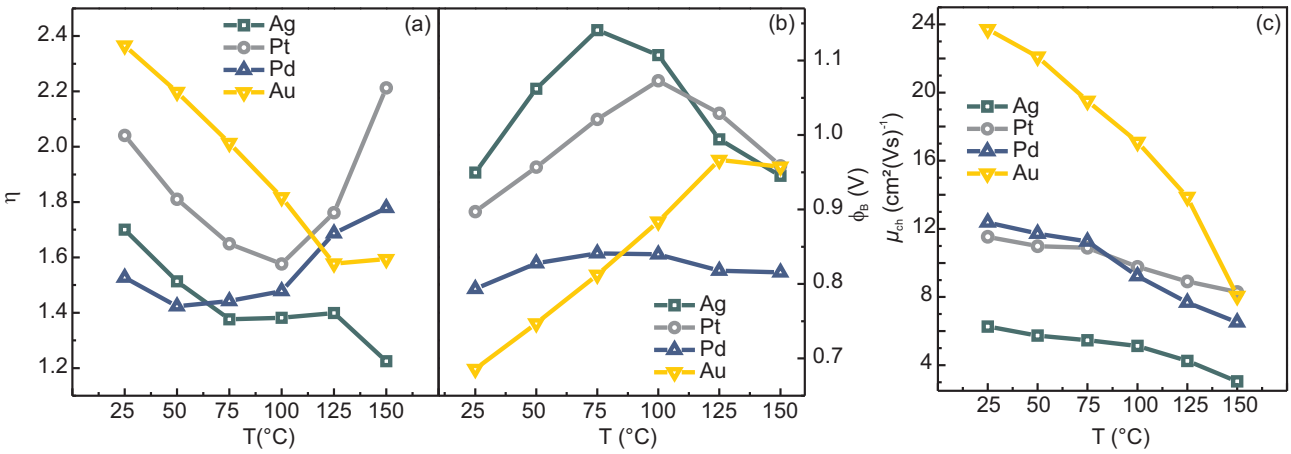


Figure 5.13: a) Ideality factor, b) Schottky barrier height and c) Channel mobility of various metal-gate MESFET at elevated temperatures.

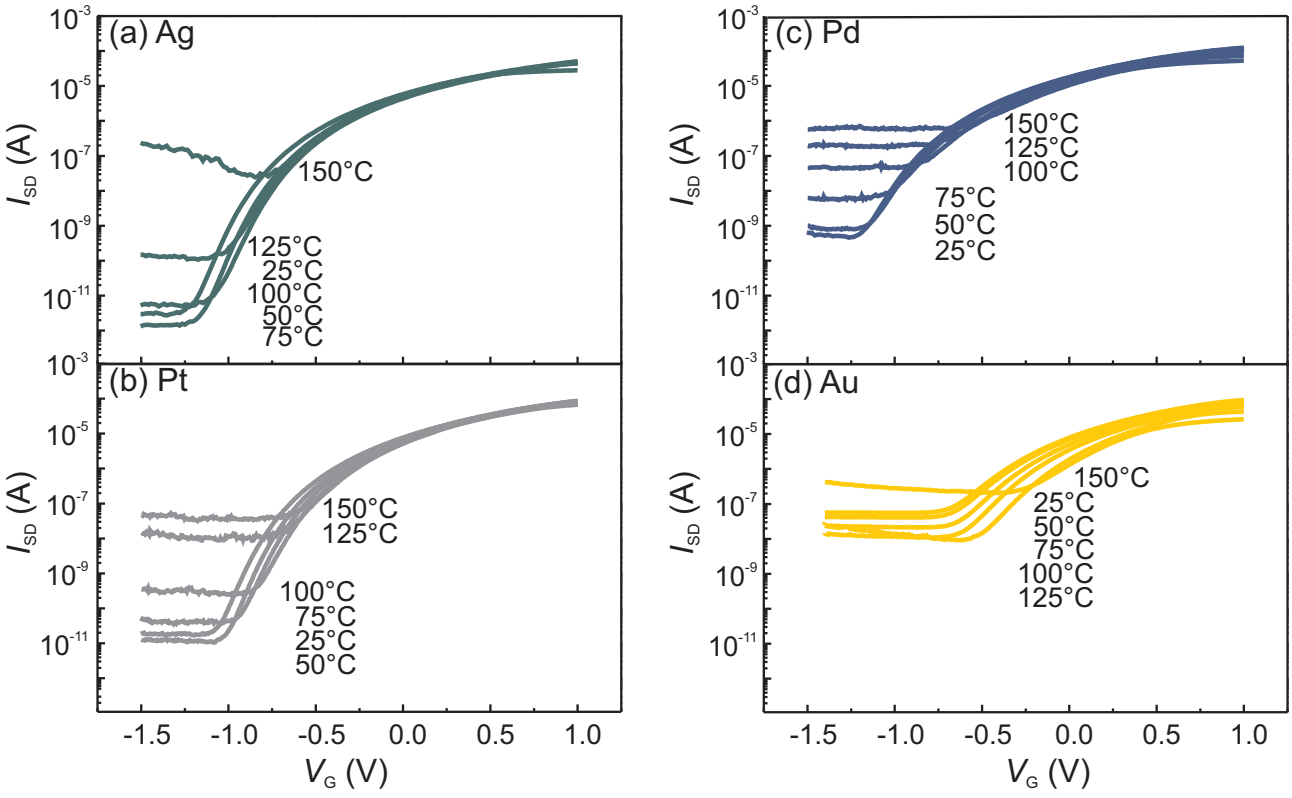


Figure 5.14: Transfer characteristics of MESFET with a) Ag, b) Pt, c) Pd, and d) Au Schottky-gate contact at elevated temperatures.

much higher gate leakage currents leading to a faster degradation of the MESFET with increasing temperatures.

Based on the results of the gate metal comparison, Ag-gate MESFET are still suggested to be used as standard for further investigations. Although the Ag-MESFET had the smallest channel mobility, the other electrical properties such as ideality factor, Schottky barrier height, on/off-ratio, and off-current are the best. However, Pt is an alternative, since it shows similar electrical performance as Ag.

Bias stress and light exposure

For additional reliability evaluation, bias stress measurements have been performed on MESFET with Ag-gates (Fig. 5.15). This FET showed an initial on/off-ratio of 1.0×10^8, a channel mobility of 8.3 cm^2/Vs, and turn-on voltage of −1.27 V. It is known from MISFET technology that a shift of the turn-on voltage can occur during bias stress due to charging of traps at the interface between gate insulator and semiconductor channel [Gö07a]. To minimize the influence of ambient light, the MESFET sample was kept in darkness for one week before measurement. First, a positive gate voltage of $V_G = 1$ V and a source-drain voltage of $V_{SD} = 2$ V was applied to the FET for an overall time of 79000 seconds (≅ 22 hours). Under these conditions, the channel is completely open and the maximum saturated source-drain current of 100 μA flows through the channel. Every 1000 seconds, a transfer characteristic (Fig. 5.15a) was recorded; the off-current and apparent channel mobility are depicted in Fig. 5.15b as a function of stress time. The characteristics of the MESFET did not change within the first 22 hours of positive gate stress: no shift of the turn-on voltage was observed, the off-current stays constant, and the channel mobility only slightly decreases from 8.3 cm^2/Vs to 8.0 cm^2/Vs. This indicates a secure long-term performance of the MESFET under high-power conditions. As expected from the missing insulator in the MESFET, there is no influence of interface traps, i.e. a shift of the turn-on voltage, as it is the case in MISFET, was not observed. In the subsequent measurement, negative-gate stress ($V_G = -1$ V, $V_{SD} = 2$ V) was applied for another 22 hours. Here, the depletion region under the gate is almost fully expanded and only a source-drain current of 1 nA flows. As can be seen in Fig. 5.15b, the off-current decreases immediately by one decade resulting in an on/off-ratio in the range of 10^9. The channel mobility drops to a mean value of 3.0 cm^2/Vs. After the fast (within a few seconds) initial change, both values remain constant during the rest of the stress time. After this measurement, the microscope light of the used waferprober (150 W metal halide lamp) was turned on for a few seconds before the MESFET was again measured in darkness but without voltage stress for 10000 seconds. During this time, the off-current is constantly one order of magnitude higher than the initial value indicating persistent photo conductivity. The channel mobility is again at 8.0 cm^2/Vs. Finally, negative-gate stress ($V_G = -1$ V, $V_{SD} = 2$ V) was applied again and the on/off-ratio is immediately restored to a mean value of 3.0×10^8. The channel mobility is monotonically decreasing to a value of 5.8 cm^2/Vs within 15000 seconds.

The behavior of the MESFET during bias stress leads to the assumption that there is a persistent photo conductivity mechanism in the ZnO channel. For the positive-gate stress, there is no depletion layer under the gate. Under these conditions, the source-drain-field alone is not strong enough (~ 0.3 kV/cm) to charge or discharge a corresponding trap in the channel. No change in the MESFET conductivity is observed. With a negative voltage applied at the gate the accumulation of the source-drain field and the field due to the Schottky contact's depletion region is strong enough for carriers to

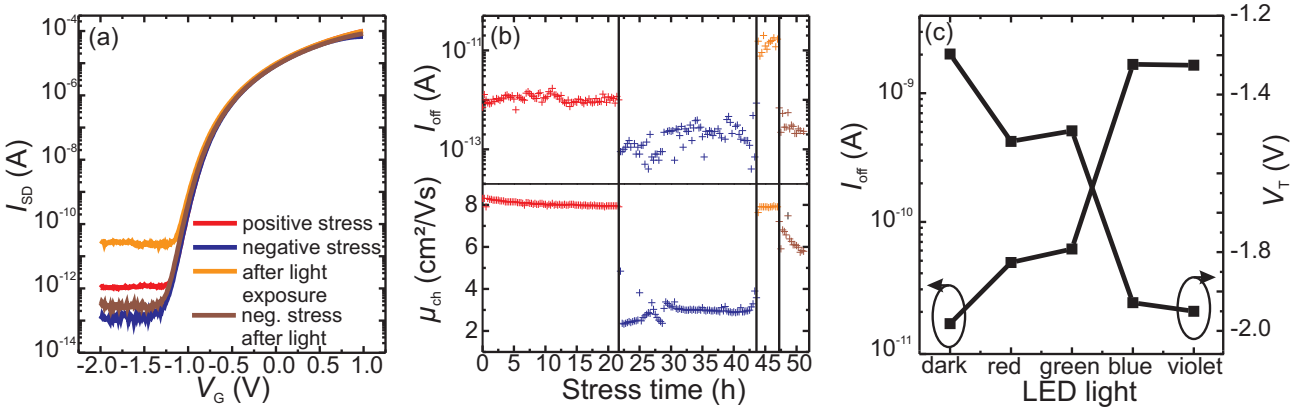


Figure 5.15: a) Transfer characteristics of a Ag-gate ZnO MESFET during bias stress and after exposure of visible light. b) Corresponding off-current and mobility. c) Off-current and turn-on-voltage of a ZnO-MESFET under exposure of different colored light.

overcome a trap barrier and charge or discharge. This leads to an altered conductivity in the channel. The off-current as well as the forward transconductance (and the apparent channel mobility) of the MESFET are reduced. Turning the light on restores the traps' charge state, which again remains constant over a longer period of time (10000 s) in darkness. By applying negative gate-voltage stress again, the conductivity of the channel decreases again, however, with a longer time constant.

In order to elucidate the impact of light irradiation on the MESFET parameters, the devices were consecutively exposed to light of different-colored LEDs with wavelengths of 625 nm (red), 525 nm (green), 470 nm (blue), and 425 nm (violet), respectively. The intensity of the LEDs was adjusted to 1 mW/cm^2, measured using a *HP8153A lightwave multimeter* equipped with an optical Si-diode head. After setting up the measurement, the sample was first kept in darkness for 5000 s and a transfer characteristic was recorded every 500 s. The characteristic did not change during this time: $I_{off} = 1.7 \times 10^{-11}$ A, $V_T = -1.30$ V, $\mu_{ch} = 7.8$ cm^2/Vs. Then, the sample was exposed to red light (Fig. 5.15c) for 8000 s. Immediately (within the first 500 s), the off-current slightly increased to $I_{off} = 4.8 \times 10^{-11}$ A and the turn-on voltage shifted to $V_T = -1.52$ V and stayed constant for the rest of the stress time. Under green-light exposure, these values remained in the same range. However, under blue and violet light, I_{off} and V_T changed drastically to 1.7×10^{-9} A and -1.95 V, respectively. The changes in these parameters are due to the photo-generated charge carriers, which reduce the expansion of the depletion region. The charge carriers originate from defect states within the energy band gap of ZnO (365 nm). With increasing photon energy from red to violet the probability of inter-band transitions increases exponentially. All light-induced changes in the transfer characteristics of the MESFET were completely reversible and no persistent photo conductivity was observed in this sample after the light was turned off. This is contrary to the observations that were made on zinc tin oxide MISFET [Gö07b] under the illumination with visible light. Under irradiation with violet light, threshold-voltage shifts between 2 V and 20 V were observed (compared to maximum 0.65 V in the here presented MESFET) depending on the processing temperature and the zinc/tin-composition. Moreover, Görrn *et al.* described a time constant for the recovery of the turn-on voltage in the order of 20 hours [Gö07b]. These differences between MISFET and MESFET can be attributed to the

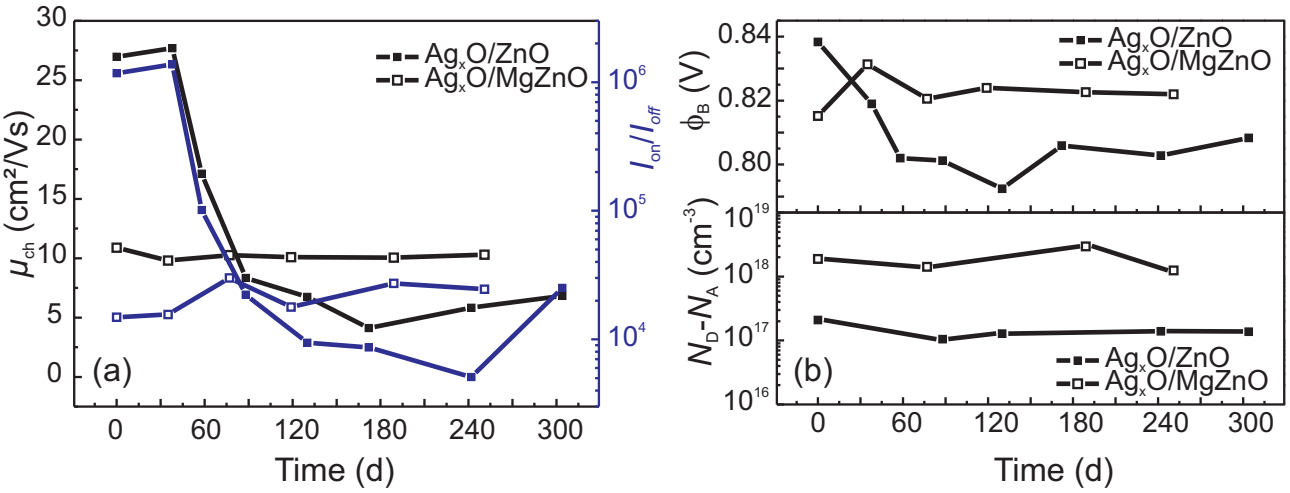


Figure 5.16: Long-term stability of a) the channel mobility and on/off-ratio b) the Schottky barrier height of the gate and net doping concentration of ZnO- and MgZnO-channel MESFET.

insulator/semiconductor interface. The turn-on voltage shift in MESFET is much smaller, because the charge trapping in the dielectric is dismissed; only the creation of defects in the channel volume material contributes to this effect.

Long-term stability

Figure 5.16 depicts a comparison of long-term stability measurements between MESFET with ZnO channel grown as described in Sec. 3.1 and a channel that comprises ZnO with a small amount (0.25%) of Mg. The samples were both equally processed without any encapsulation and stored in an exsiccator at room temperature and under ambient air and light. Transfer and Schottky characteristics were recorded in intervals of several weeks. For the ZnO-channel, the measurements reveal (Fig. 5.16a), that the channel mobility and on/off-ratio remained constant for the first 40 days at their initial values of 27 cm^2/Vs and 1.3×10^6, respectively. After that, both parameters rapidly began to decrease and saturated at values in the range of $\mu_{ch} \sim 5\,cm^2$/Vs and $I_{on}/I_{off} \sim 10^4$. On the other hand, the initial channel mobility and on/off-ratio of the MgZnO channel is only 10 cm^2/Vs and 2×10^4, respectively. However, it stays constant over the whole measurement period of 250 days. Measurements of the Schottky-gate contacts reveal (Fig. 5.16b) that the net doping concentration $N_D - N_A$ stays constant for both samples; i.e. a diffusion of Ag from the gate contact does not lead to compensation and is not responsible for this effect[Wen10a]. Instead, the Schottky barrier height of the gate contacts decreases for the sample with ZnO-channel, whereas it stays constant for the ZnMgO-channel. The decrease of the Schottky barrier height from 0.84 V to 0.8 V is consistent with the decrease of the forward transconductance (and the channel mobility) by a factor of five. This leads to the conclusion that the degradation of the gate contact is more pronounced for the pure ZnO-channel.

Table 5.7: Overview of the measured MESFET properties on quartz for various Al-contents in the target.

Al-content (wt-%)	d (nm)	$N_D - N_A$ (10^{17} cm^{-3})	V_T (mV)	μ_{ch} (cm^2/Vs)	on/off-ratio (10^4)	S_{min} (mV/decade)
undoped	28	1.0	470	0.07	1.7	63
0.001	28	13.6	-5	0.10	9.6	135
0.01	25	5.5	-7	0.32	46.1	120
0.05	28	35.0	-240	0.24	14.0	144
0.1	28	2.6	160	0.02	4.4	106

5.2 Glass substrate

For the use of ZnO MESFET technology in future low-cost transparent electronics, it is of great interest to fabricate those devices on glass substrates, which are cheaper and more easily scalable than the previously used sapphire substrate. In this section, properties of MESFET on different glass substrates are presented. This work is done in collaboration with Michael Lorenz (Universität Leipzig), who performed structural and electrical measurements of MESFET on glass within his diploma thesis [Lor09].

5.2.1 Growth parameters of ZnO thin films on quartz glass

The growth of a ZnO channel layer on amorphous glass substrates leads to a higher density of structural defects like dislocations, twist and tilt of grains, and higher surface roughness compared to the growth on sapphire substrates. Furthermore, similar to the growth on sapphire, the electrical properties of such ZnO thin films are affected by the diffusion of elements from the substrate during growth. Therefore, the influence of PLD growth parameters on the structural and electrical properties of ZnO channel layers are investigated. At first, this is done on quartz glass substrate, before various glass substrates are compared in Sec. 5.2.2.

Figure 5.17 depicts the full width at half maximum (FWHM) of the ZnO (0002) peak obtained from XRD ω-scans and the root-mean-square (rms) surface roughness of ZnO channel layers obtained by AFM in dependence on the substrate temperature T_S (Fig. 5.17a) and the oxygen partial pressure p_{O_2} (Fig. 5.17b) during PLD growth. It can be seen from Fig. 5.17a, that with increasing T_S the ω-FWHM increases due to decreased c-orientation of the ZnO crystals. An increasing 2θ-FWHM (not shown) means a decreasing size of the crystals. A further decrease of T_S below 625°C leads to a further alignment of the grains but not to larger grains. Additionally, the rms surface roughness is increasing with higher temperatures. The dependence on the oxygen partial pressure (Fig. 5.17b) shows, that the best crystal quality is achieved for $p_{O_2} = 0.016$ mbar; i.e. rms-roughness and ω-FWHM are low.

From these results, ideal growth parameters are assumed to be low substrate temperatures $T_S < 625$°C and an oxygen partial pressure of $p_{O_2} = 0.016$ mbar. However, as Fig. 5.18 shows, the channel mobility of MESFET is decreasing with increasing p_{O_2} and T_S. Higher resistances limit the maximal current in the on-state of the transistors. A possible reason for this is a lower concentration of donor-like zinc interstitials for higher oxygen partial pressures [Zha01]. For that reason, the growth parameters $T_S = 675$°C and $p_{O_2} = 3 \times 10^{-4}$ mbar are used for further investigations of ZnO-MESFET on glass

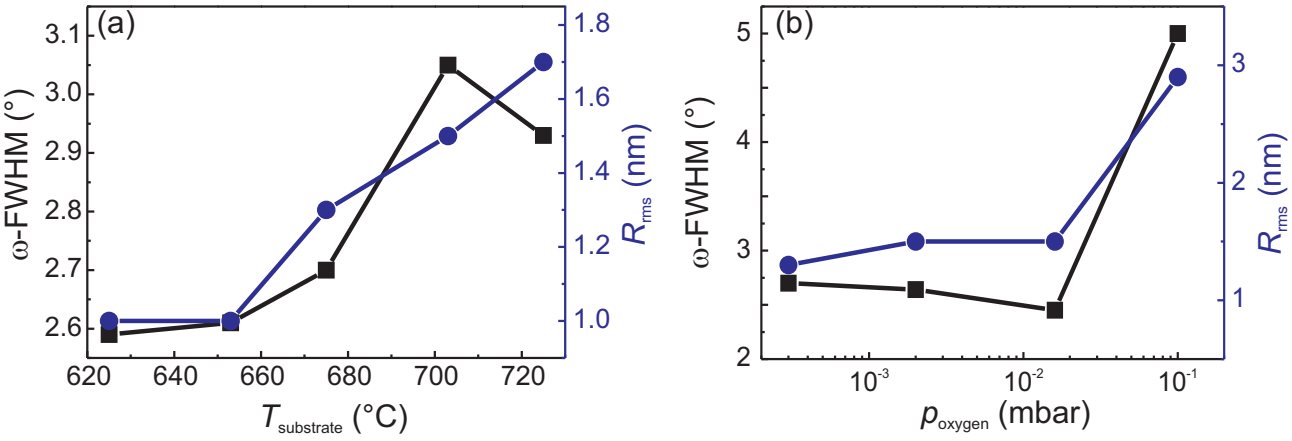


Figure 5.17: XRD ω-scan FWHM of the ZnO (0002) peak and rms surface roughness (AFM) of ZnO channel layers ($d \sim 30$ nm, ZnO:Al(0.01 wt-%)) on quartz glass in dependence of a) substrate temperature and b) oxygen partial pressure.

substrates. With these parameters, a variation of the Al-content in the PLD target for the growth of the ZnO channel is investigated. Tab. 5.7 summarizes the measured MESFET properties. The undoped sample has the lowest net doping concentration of 1.0×10^{17} cm^{-3}, which probably comes from intrinsic donors such as zinc interstitials. Its positive turn-on voltage of $V_T = +470$ mV is the highest observed for MESFET within this thesis resulting in the lowest minimum slope $S_{min} = 63$ mV/decade. However, the on/off-ratio of 10^4 and low channel mobility of 0.07 cm^2/Vs makes this MESFET not suitable for further applications. Also the MESFET with 0.1 wt-% Al has a high turn-on voltage but very low channel mobility and on/off-ratio. Here, a similar effect occurs like in the discussion of Fig. 5.6. Higher Al-contents are not incorporated as donors in the ZnO matrix. Most likely the Al accumulates at structural defects such as grain boundaries. Since the highest mobility and on/off-ratio is achieved for 0.01 wt-% Al, this is chosen to be the standard doping for ZnO MESFET on glass substrates.

5.2.2 Comparison of various glass substrates

The influence of various glass substrates on the structural quality of ZnO thin films and electrical properties of MESFET thereon were investigated [Fre09c]. Three different glass substrates are considered: $10 \times 10 \times 1$ mm^3 quartz glass (*Crystal Berlin*), $10 \times 10 \times 0.7$ mm^3 borosilicate 1737 (*Corning*), and $10 \times 10 \times 0.7$ mm^3 borosilicate Eagle XG (*Corning*) [Vin00, Cor02, Cor06]. In contrast to quartz consisting of pure silicon oxide, the latter two substrates are borosilicate glasses which consist of alkaline earth boro-aluminosilicates and are commonly used for the fabrication of flat-panel displays. The difference between the two *Corning* glasses is, that for Eagle XG no heavy metals are used during the fabrication process and the thermal expansion is reduced compared to 1737. The borosilicate substrates are approximately one third cheaper than quartz substrates and are easily scalable to sizes of several square meters.

At first, the structural properties and chemical composition of the glass substrates are investigated. Figure 5.19 depict AFM measurements of the surface of as-received quartz and borosilicate substrates.

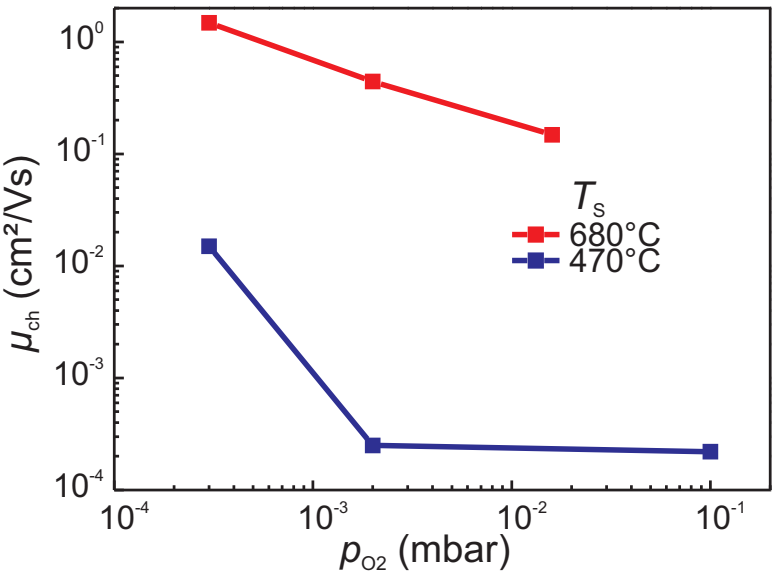


Figure 5.18: Channel mobility of ZnO-MESFET on quartz glass in dependence of substrate temperature and oxygen partial pressure.

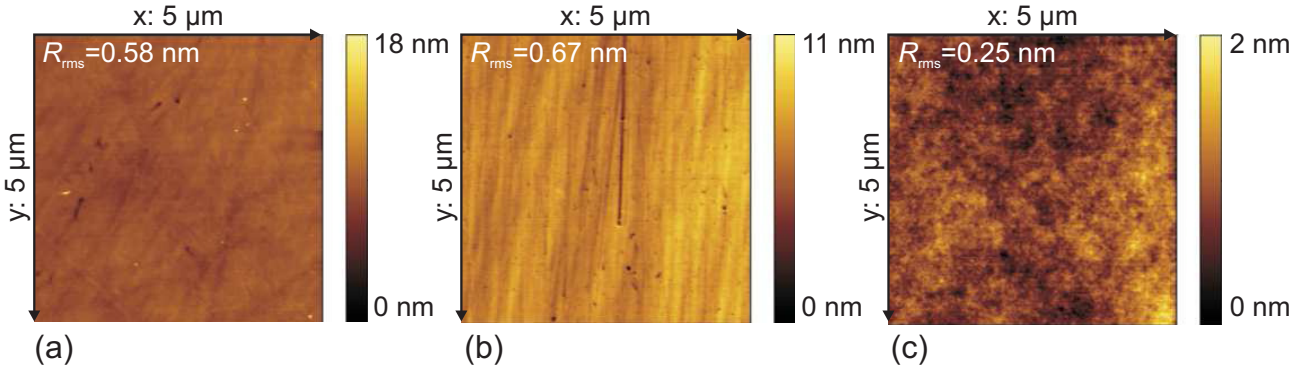


Figure 5.19: AFM pictures of the surface of a) Quartz, b) Corning 1737, and c) Corning Eagle XG substrates.

All three glasses show an amorphous surface with no grains. The rms-roughnesses are R_{rms} = 0.58 nm, R_{rms} = 0.67 nm, and R_{rms} = 0.25 nm for quartz, 1737 and XG, respectively. Quartz showed some polishing damages that are up to 10 nm deep and do not have a preferred direction. On the other hand, 1737 showed polishing damages that have a clear preferred direction but are not as deep as for quartz. XG did not show any surface structure or polishing damages. Annealing of the substrates with the polishing damages for 30 minutes at p_{O_2} = 800 mbar and temperatures between 790°C and 870°C lead to an accumulation of material at the damages. They were not reduced and the surface roughness was increased. For that reason, within this thesis, as-received substrates are used for the fabrication of MESFET.

XRD 2θ-ω-scans were performed on the glass substrates (Fig. 5.20). Although the glasses are amorphous, they show a broad peak with low intensity due to constant bonding distances and coordination of the silicon and oxygen atoms. The distances from the peak positions are 4.1 nm, 3.6 nm, and

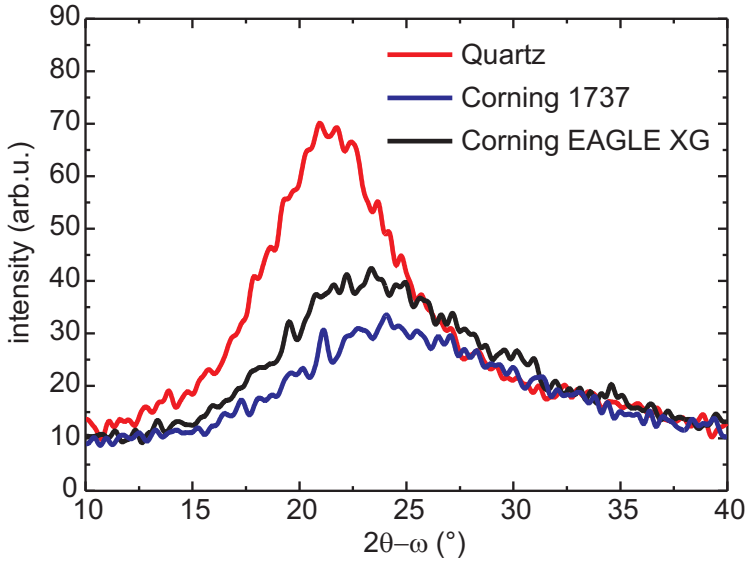


Figure 5.20: XRD 2θ-ω-scans of glass substrates (10-point FFT-smoothed).

3.8 nm for quartz, 1737 and XG, respectively. For quartz, it coincides with theoretical calculations and measurements of Warren [War37]. The borosilicate glasses 1737 and XG show lower intensities and higher scattering angles compared to quartz. This is due to the incorporation of additional atoms like aluminium or boron, which alters the ratio of silicon and oxygen and reduces their bonding distances.

Energy-dispersive X-ray spectroscopy (EDX) measurements were performed by J. Lenzner (Universität Leipzig) on glass substrates (Fig. 5.21). A multitude of foreign impurity atoms was found within the glass substrates. In quartz, iron (Fe), tin (Sn) and thallium (Tl) are incorporated. However, more elements such as magnesium (Mg), aluminium (Al), calcium (Ca) and strontium (Sr) were found in the borosilicates, which has an effect on the electrical properties of the ZnO thin films on these substrates. Additionally, secondary-ion mass spectroscopy time-of-flight (SIMS-tof) measurements were performed by S. Richter (Fraunhofer Center of Silicon Photovoltaic (CSP), Halle) on samples, where ZnO thin films were grown on glass substrates and for comparison on sapphire. The analysis of elements that tend to form compensating defects are summarized in Tab. 5.8. It can be seen, that the amount of lithium (Li), sodium (Na), potassium (K) and boron (B) is dramatically increased in the glass substrates compared to sapphire. However, the diffusion of these elements into the ZnO thin film is not distinctive. Li and B seem to play no role; their detected intensities in the substrates is hardly exceeding the detection limit. On the other hand, more Na and K are incorporated in ZnO films on glasses compared to sapphire. Films grown on Eagle XG contain the highest amount of Na and K.

ZnO thin films were grown with the above found standard PLD growth parameters on glass substrates and on a sapphire substrate. Note, that the standard growth parameters for MESFET on sapphire differ from that on glass. However, the standard parameters for glass were used in this case also for sapphire (except, that a pure ZnO target was used for sapphire since the Al doping is generated by diffusion from the substrate) in order to compare the influences of the glass substrate on the MESFET

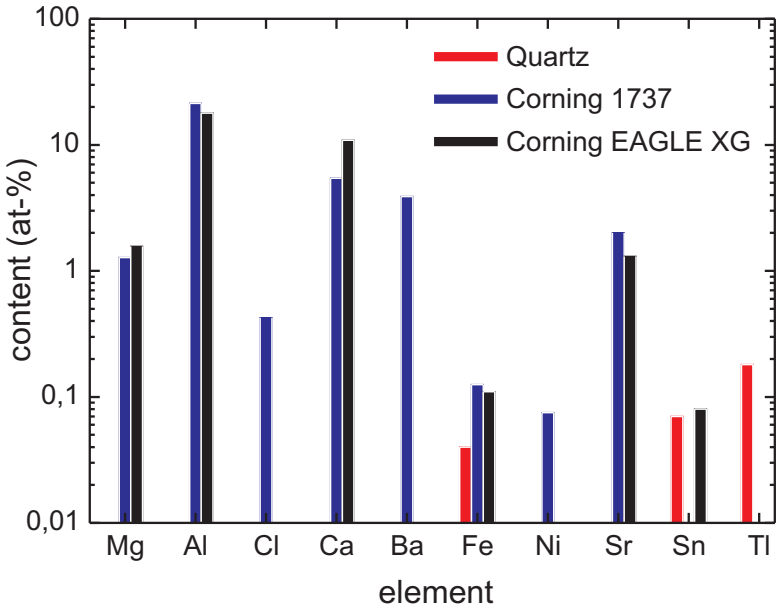


Figure 5.21: Contaminats of the glass substrates measured by EDX. (The measurements were performed by J. Lenzner, Universität Leipzig.)

Table 5.8: TOF-SIMS analysis (positive polarity) of ZnO thin films and various substrates. The measurements were performed by S. Richter (Fraunhofer CSP, Halle). The noise level was at an intensity of ~ 0.1 counts.

	Intensity of elements (counts)			
	Li	Na	K	B
substrates				
Quartz	15	1500	1500	25000
1737	20	1800	2000	30000
Eagle XG	18	650	2000	35000
Sapphire	< 1	2	2	< 1
ZnO film on				
Quartz	1	4	5	1
1737	< 1	3	4	2
Eagle XG	< 1	10	20	1
Sapphire	1	2	2	< 1

performance.

AFM measurements of the ZnO channel surface on sapphire and glass substrates showed differences in the morphology. Figure 5.22a depicts such AFM measurements for sapphire and quartz glass; the morphology of the thin film on quartz and the borosilicates are similar. On glass, a Volmer-Weber island growth [DBC94] is observed; i.e. the interaction between atoms of the film on the surface is larger than the interaction between atoms of the film and the substrate. On the other hand, on sapphire, an epitaxial relation between film and substrate exists. A mixed mechanism between Franck-van-der-Merwe film growth [DBC94] and island growth occurs. The grain sizes on the glass substrates lie in the range between 30 and 50 nm. The rms-roughnesses of the channel surface on the glass substrates

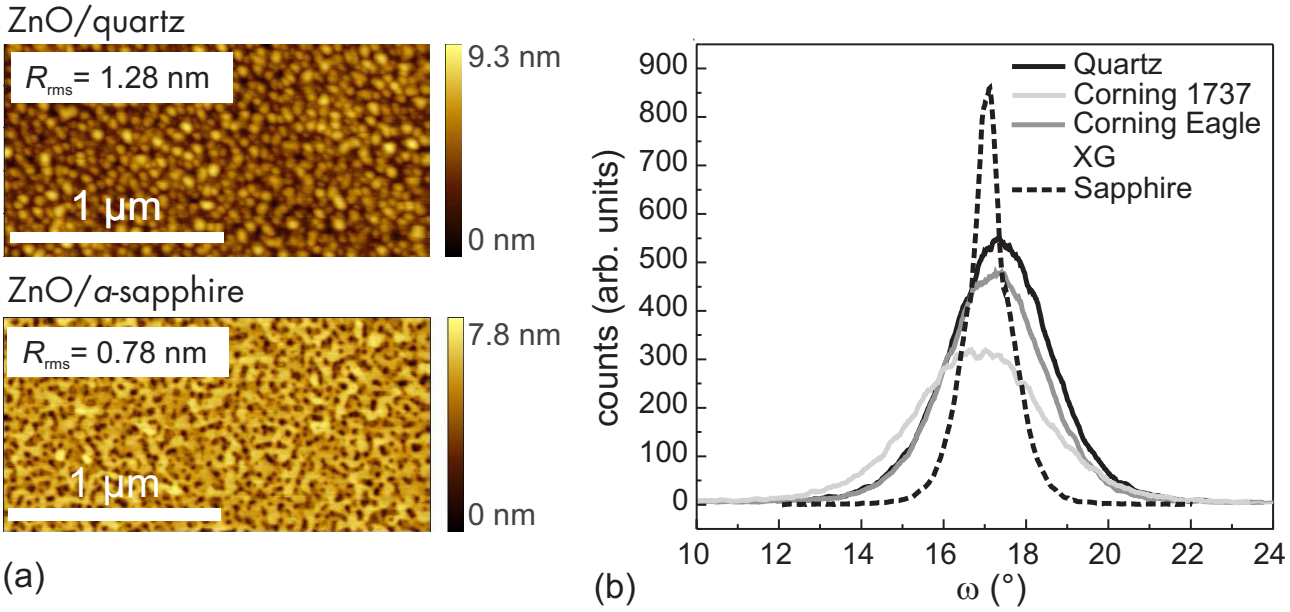


Figure 5.22: a) AFM pictures of a ZnO MESFET channel layer on quartz glass and *a*-sapphire substrate. b) XRD ω-scans of the ZnO-(0002) peak on various glass substrates and sapphire.

Table 5.9: Structural and morphological parameters of ZnO MESFET channels on glass and sapphire.

Substrate	FWHM XRD-ω (°)	AFM-rms (nm)
Quartz	2.74	1.28
1737	3.60	1.46
Eagle XG	2.81	1.38
Sapphire	0.95	0.78

is increased compared to sapphire (Tab. 5.9). The FWHM of the ZnO (0002) peak on glass substrates in XRD ω-scans (Fig. 5.22b) is significantly higher than that on sapphire. Due to the amorphous substrates, the mocaicity of the ZnO thin film on the glass substrates is lower than for the film on sapphire. However, no additional peaks from other orientations or crystal phases have been observed in XRD measurements.

Figure 5.23 compares Schottky-gate characteristics of MESFET on glass and sapphire substrates. It is noticeable, that the reverse currents of the diodes on glass are one to two orders of magnitude lower than for the diodes on sapphire. The diode on glass still reach about the same forward current resulting in higher rectification ratios at ±2 V. The results of the modelling of the diode characteristics are summarized in Tab. 5.10. All diodes achieve an ideality factor of 1.7, which is comparable to the MESFET grown with standard parameters on sapphire substrate. The Schottky barrier heights are increasing from quartz over 1737 to Eagle XG, which almost reaches the value of sapphire.

Figure 5.24a exemplarily depicts the output characteristics of a ZnO MESFET on quartz. All MESFET on glass and on sapphire show similar behavior. Clear saturation with almost ideally constant saturation current is observed for small V_{SD} range between 0 V and 2 V. Breakdown did not occur

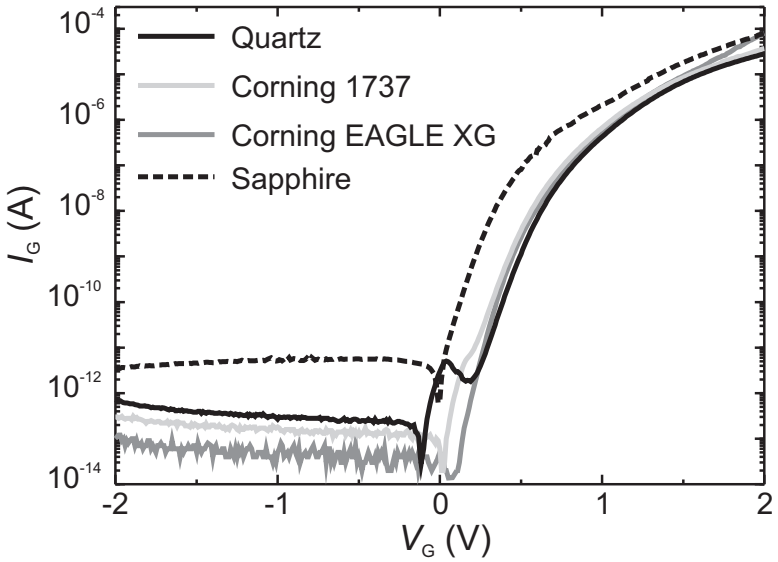


Figure 5.23: IV characteristics of the Schottky-gates of MESFET on various glass substrates and sapphire.

Table 5.10: Properties of the gate diodes of MESFET on various glass substrates and sapphire.

Substrate	rect.-ratio at ±2 V	R_S (kΩ)	Φ_B (V)	η
Quartz	3.9×10^7	20	0.89	1.7
1737	1.2×10^8	14.4	0.91	1.7
Eagle XG	6.6×10^8	4.7	0.94	1.7
Sapphire	2.3×10^7	6.5	0.95	1.7

until 5–8 V. Compared to the MESFET on sapphire (Sec. 5.1), the source-drain currents were in the lower micro ampere range. For high gate voltages in the vicinity of the flat-band condition (near 1 V), a shift of the output characteristic occurs due to the increasing gate currents, as it was also observed for MESFET with different gate materials in Sec. 5.1.

The transfer characteristics of the MESFET are shown in Fig. 5.24b. In contrast to the MESFET on sapphire (Sec. 5.1), all MESFET on glass substrates as well as the MESFET on sapphire, grown with standard parameters for glass, are normally-off. They have threshold-voltages of $V_T = 0$ V for quartz, +170 mV for 1737, and +340 mV for XG, respectively. An overview of the measured MESFET parameters is given in Tab. 5.11. The net doping concentration $N_D - N_A$, obtained from QSCV measurements, is in the range of 10^{17} cm^{-3}, which is one order of magnitude lower than for the standard MESFET S3 on sapphire (Tab. 5.4). Hall-effect measurements on the MESFET on glass did not show a conclusive result due to the high resistance of the thin ZnO films. As the turn-on voltage increases for the respective glass substrates, the on-current decreases by two orders of magnitude resulting in lower on/off-ratios. On the other hand, the minimum slope S_{min} decreases for the glass MESFET with higher positive threshold voltages. The slope for sapphire is comparable to the values presented in Sec. 5.1.

As can be seen in Tab. 5.11, the channel mobility is highest for the sapphire reference sample

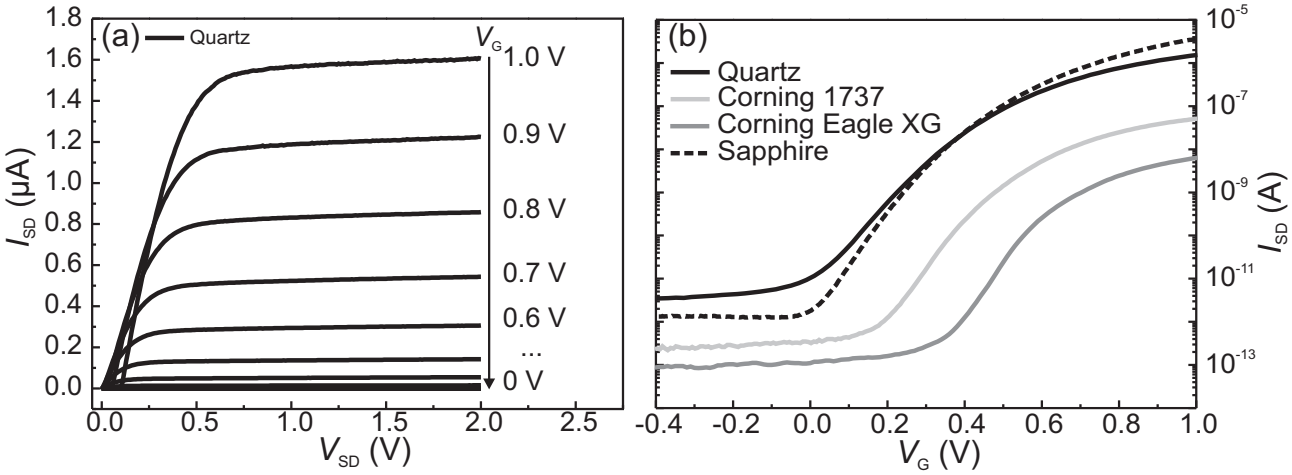


Figure 5.24: a) Output characteristic of a ZnO MESFET on quartz glass substrate. b) Transfer characteristics of ZnO MESFET on various glass substrates and sapphire.

Table 5.11: Overview of the measured properties of MESFET on various glass substrates.

Substrate	d (nm)	$N_D - N_A$ (10^{17} cm^{-3})	V_T (mV)	μ_{ch} (cm^2/Vs)	on/off-ratio (10^5)	S_{min} (mV/decade)
Quartz	30	5.7	0	1.30	4.7	125
1737	25	1.8	170	0.22	2.3	101
Eagle XG	24	1.3	340	0.04	0.8	104
Sapphire	15	1.3	0	25.0	26.9	77

(25 cm^2/Vs). It decreases by one order of magnitude for glass (1.3 cm^2/Vs), and by another one and two orders of magnitude for 1737 (0.2 cm^2/Vs) and XG (0.04 cm^2/Vs), respectively. Apparently, this is due to the decreasing on-current as the turn-on voltage increases for the respective glass substrates. The lower I_{SD} is caused on the one hand by higher gate leakage currents, which reduce the forward transconductance and thus the channel mobility obtained from Eqn. 2.54. On the other hand, the electron mobility is reduced on amorphous substrates due to scattering at grain boundaries incorporated in much higher density. This is clear comparing the AFM pictures in Fig. 5.22a. The island growth on glass leads to a larger amount of high-angle grain boundaries, whereas the closed-film growth on sapphire has more percolating paths in the channel and less high-angle grain boundaries resulting in a higher mobility.

The higher resistances and lower currents of MESFET on glass substrates indicate the influence of compensating defects. It is known from TOF-SIMS measurements (Tab. 5.8), that such defects exist in the substrates and diffuse into the channel layer during growth. In order to clarify and compare the presence of defects in the ZnO films grown on the different substrates, room-temperature admittance measurements (AS) were performed on Schottky diodes deposited under identical growth parameters as the MESFET but with a thickness of 150 nm. The larger thickness was used to reduce the influence of the series resistance and to ensure that the SCR can be modified without pinch-off at the substrate.

Figure 5.25 depicts admittance spectra and normalized conductivity spectra for the Schottky diodes on

glass substrates and the reference on sapphire. The capacitance for the diode on sapphire (Fig. 5.25a) remains constant up to an angular frequency of $\omega = 5 \times 10^6\,\mathrm{s}^{-1}$ before it decreases rapidly. The corresponding conductivity spectrum (Fig. 5.25b) shows a clear peak for $\omega = 2.2 \times 10^5\,\mathrm{s}^{-1}$, which can be assigned to the defect E3 typically observed in ZnO [Wen08]. The series resistance limits the measurement for frequencies above $6 \times 10^6\,\mathrm{s}^{-1}$. For the diode on quartz glass, the AS measurement (Fig. 5.25c, d) did not show a single defect, but the constant negative slope indicates that there is a broad distribution of deep defects. The cutoff frequency is similar to that of the sapphire sample. ZnO on 1737 glass has an admittance spectrum (Fig. 5.25e,f) similar to the sample on sapphire. In the normalized conductance spectra, peaks occured, which can be related to defects with a defined emission rate. However, the cutoff frequency is much lower (around $10^5\,\mathrm{s}^{-1}$). For XG (Fig. 5.25g, h), the decreasing capacitance is only due to the high series resistance with a cutoff frequency around $10^4\,\mathrm{s}^{-1}$. These observations indicate a large amount of deep defects in the ZnO films on glass. However, due to the comparatively low cutoff frequency, an investigation of theses diodes by means of deep-level transient spectrocopy (DLTS) was not possible, because a test frequency of 1 MHz is needed.

5.2.3 Reliability and degradation

During the investigations of MESFET on glass substrates, a fast degradation of the electrical properties has been observed. Figure 5.26a depicts transfer characteristics of MESFET, fabricated with standard parameters on quartz glass substrate, measured at the day of fabrication and several days after. It can be seen (Fig. 5.26b) that the turn-on voltage shifts in positive direction and the channel mobility is monotonically decreasing from $\mu_{ch} = 0.6\,\mathrm{cm}^2/\mathrm{Vs}$ at the first day to $\mu_{ch} = 0.1\,\mathrm{cm}^2/\mathrm{Vs}$ after 56 days. The on/off-ratio is first increasing within 3 days before it decreases by a factor of two within 56 days. The increase of the on/off-ratio can be explained by the decrease of reverse current of the gate diode (Fig. 5.26c) due to an increasing Schottky barrier height (Fig. 5.26c). However, with increasing turn-on voltage, the on-current of the MESFET decreases similar to Fig. 5.24b due to excessive gate leakage currents.

The degradation of the MESFET on glass is faster than for the ZnO-MESFET on sapphire (Fig. 5.16). The minima for negative V_T and the on/off-ratio are already reached after 10 days compared to 120 days for sapphire. However, μ_{ch} continues to decrease for the next 46 days. Contrary to the ZnO-MESFET on sapphire, the increasing Schottky barrier height and turn-on voltage for quartz implies a possible alteration of the oxidation of the Ag_xO gate material. Furthermore, the faster degradation of MESFET on glass is probably due to the channel's crystalline quality. More structural defects such as high-angle grain boundaries promote the diffusion of compensating impurities from the substrate into the channel.

For the MESFET on quartz glass substrates, in Fig. 5.23, a charging effect was observed in the Schottky diode characteristic around $V_G = 0\,\mathrm{V}$. A shift of the turn-on voltage in transfer characteristics due to this effect was not observed. However, for the normally-off MESFET on quartz, the charging influences the onset of the transfer characteristic and the off-current near V_T. Figure 5.27 depicts Schottky characteristics of a gate diode on quartz obtained for different integration times during measurement. For the shortest integration time, an increase of the gate current is observed in the gate voltage range around $V_G = 0\,\mathrm{V}$ before I_G decreases again for negative V_G. The zero-crossing of the

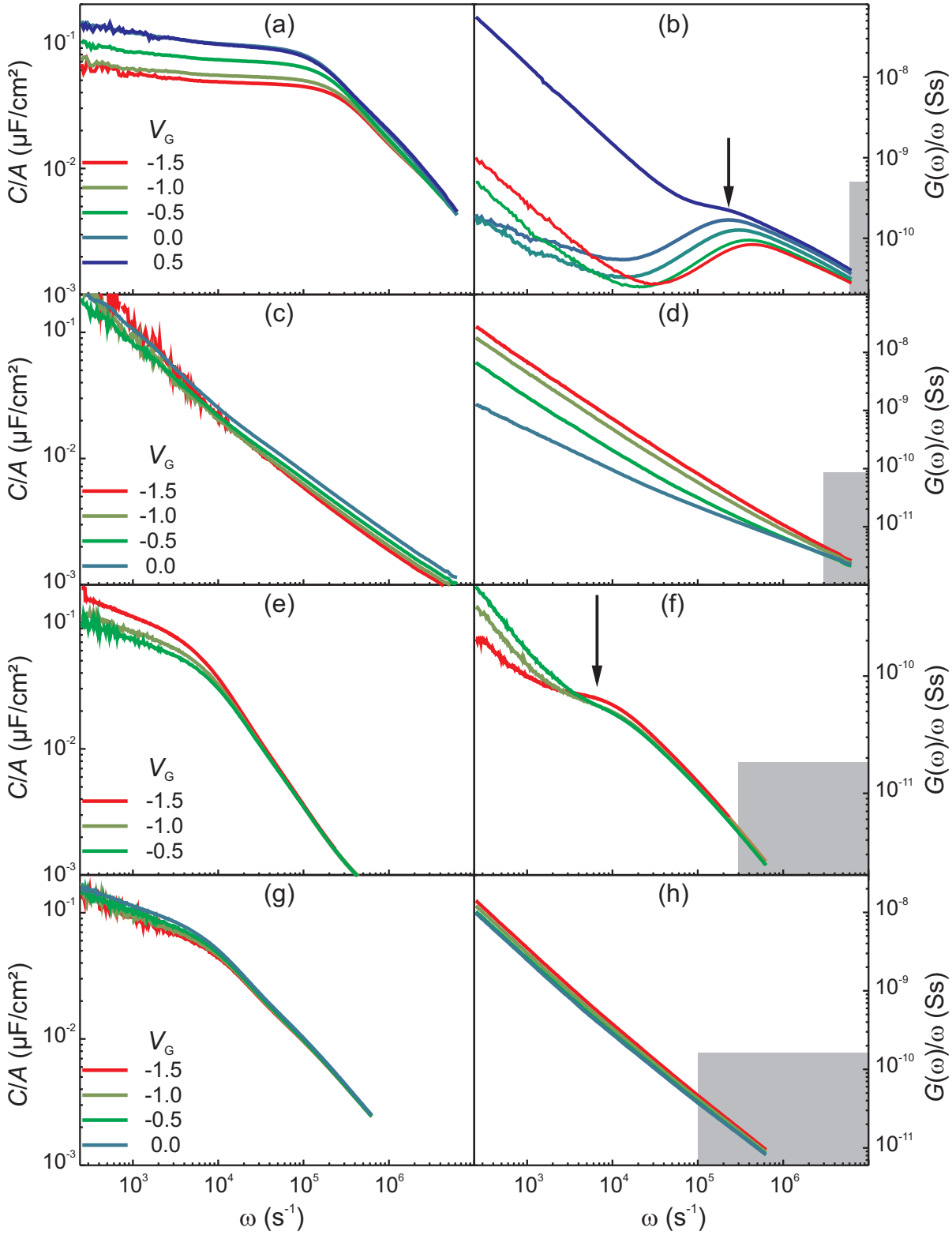


Figure 5.25: Admittance spectra of Schottky diodes on a) sapphire, c) quartz, e) Corning 1737 and g) Corning Eagle XG and b, d, f, h) corresponding normalized conductivity spectra. The arrows mark the positions of maxima; gray rectangles mark the individual cut-off frequency.

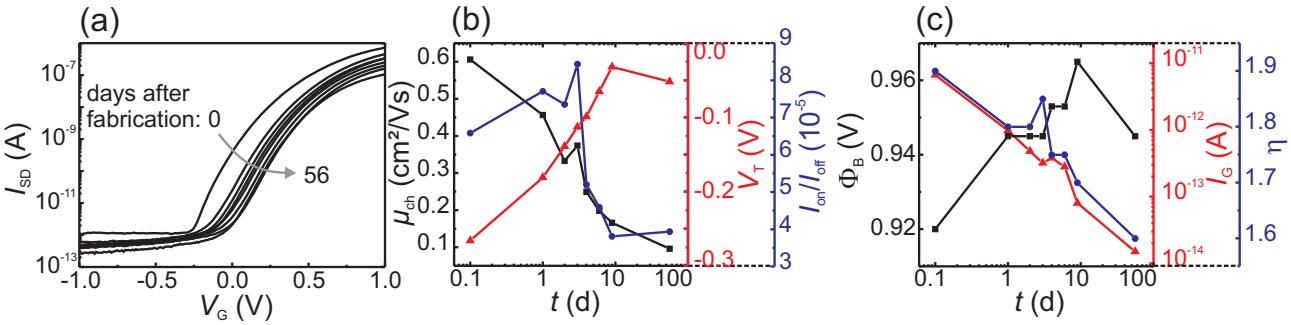


Figure 5.26: a) Transfer characteristics of a MESFET on quartz, b) μ_{ch}, on/off-ratio and turn-on voltage and c) Schottky barrier height, ideality factor and reverse current (at −1 V) of the gate diode in dependence of time after fabrication.

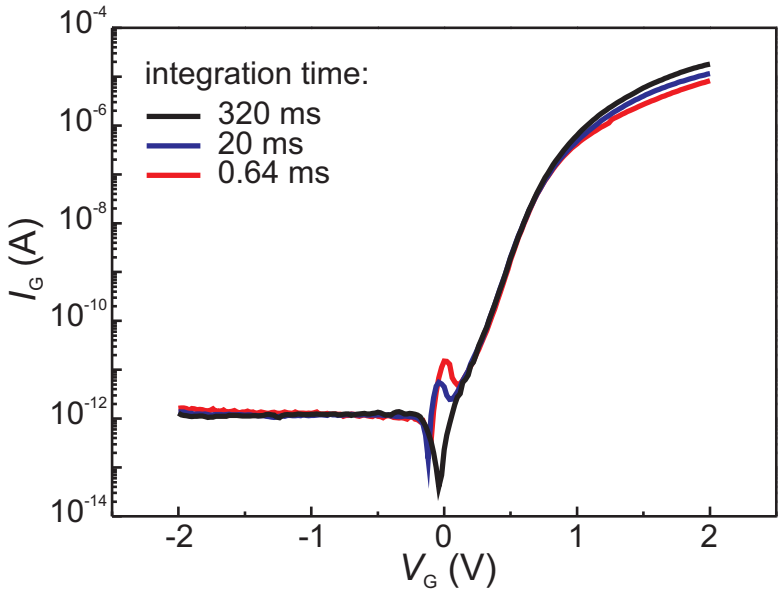


Figure 5.27: Schottky-gate characteristics of MESFET on quartz glass substrate for various integration times.

characteristic is shifted to $V = -0.12$ V. The effect of current increase is less distinctive for longer integration times, however, the zero-crossing shift is still observed. At the long integration time,the charging effect could be supressed and zero-crossing is at $V_G = 0$ V. The origin of this effect is probably an interfacial layer between the channel and the gate material, which traps charge carriers. A deeper analysis of such interface traps, as shown in Sec. 4.2.2 for MIS diodes, could not be performed because distinctive maxima in the admittance spectra (Fig. 5.25) were not observed.

The reliability of MESFET on quartz glass substrate has been investigated by means of bias stress measurements under dark conditions and under the exposure to visible light. Due to the fast degradation of MESFET on glass, a clear differentiation between stress-effect and degradation is not always possible. Therefore, the overall stress time is reduced compared to the MESFET on sapphire. Figure 5.28a depicts transfer characteristics of a MESFET with Ag-gate on quartz under bias stress with $V_{SD} = 2$ V and $V_G = 0.5$ V. Fifty transfer characteristics were recorded every 500 s; i.e. the overall

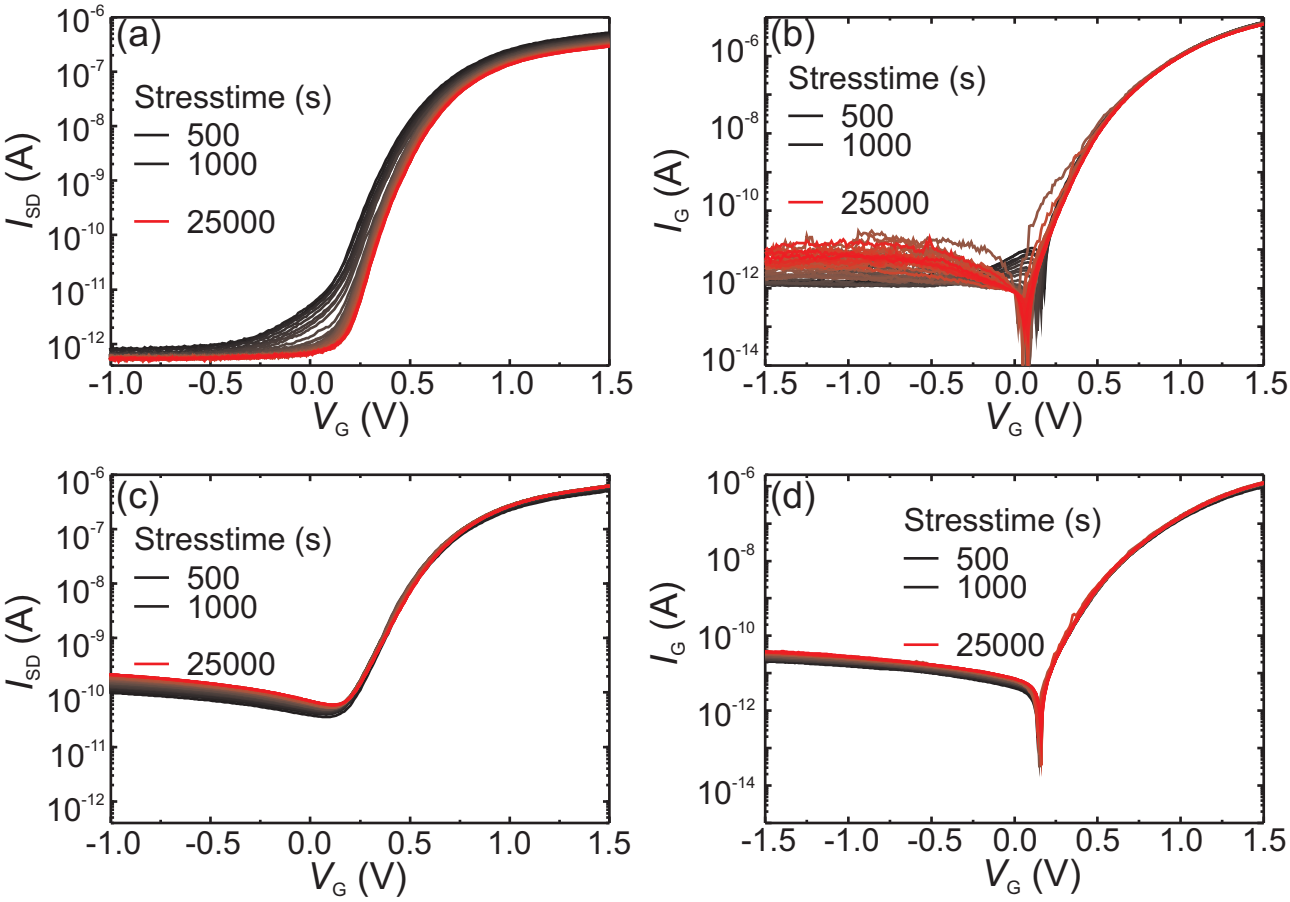


Figure 5.28: a) Bias-stress transfer characteristics measured under dark conditions, b) Corresponding gate-diode characteristics. c) Bias-stress transfer characteristics measured under exposure of visible light, d) Corresponding gate-diode characteristics.

stress time was 25000s (~ 7 h). With increasing stress time, the on- and off-current are decreasing equally, i.e. the on/off-ratio stays constant. The turn-on voltage is slightly shifting by $\Delta V_G \sim 0.2$ V in positive direction. Simultaneously, the onset of the source-drain current becomes more abrupt resulting in a steeper slope. Both effects can be explained by photoconductivity. With setting up the measurement, the MESFET sample is inevitably exposed to ambient light for a short moment. The generated charge carriers change the potential landscape below the Schottky contact and alter the transfer characteristic of the MESFET. With increasing stress time under dark conditions, the persistent photogenerated charges recombine, which results in a decrease of the net doping concentration and thus in a positive turn-on voltage shift and decrease of the source-drain current. Subsequently the measured forward transconductance is decreasing yielding a lower channel mobility of $\mu_{ch} = 0.16\,cm^2/Vs$ instead of the initial value $\mu_{ch} = 0.3\,cm^2/Vs$. The turn-on voltage shift for MESFET on glass, which was not observed for MESFET on sapphire (cf. Fig. 5.15), may be attributed to the comparably high amount of structural defects which promotes the formation of trapping charges.

Figure 5.28b shows the corresponding gate-diode characteristics for the bias stress measurements under dark conditions. With increasing stress time, an increase of the reverse gate-leakage current is

observed. However, this did not have an effect on the MESFET transfer characteristics; no change of the Schottky barrier height or ideality factor was determined by modelling the gate characteristics. Additionally, the previously described charging effect decreases and vanished after ~ 100 minutes. This indicates that the origin of this effect is the formation of deep defects at the ZnO/gate-interface.

After the bias stress measurement under dark conditions, the sample was illuminated with light from the microscope lamp of the used waferprober (150 W metal halide lamp). Under this continous illumination, the same bias stress measurements were performed. The transfer characteristics (Fig. 5.28c) show a significant increase of the off-current due to photo-conductivity. However, after 10000 s the increase in conductivity saturates. The channel mobility is increasing due to the higher forward transconductance from $\mu_{ch} = 0.2\,cm^2/Vs$ to $\mu_{ch} = 0.33\,cm^2/Vs$. A turn-on-voltage shift is not observed during this stress measurement, which implies that the traps, which caused the shift of V_T in Fig. 5.28a under dark conditions, are now discharged due to the light. The Schottky-gate characteristics under illumination (Fig. 5.28d) show a rectification ratio, which is one to two orders of magnitude lower (due to higher reverse current) than for the dark measurements. In this case, an influence of trapped charges was not observed.

The sample was kept in darkness for 45 days after the stress measurements. The measured transfer characteristic after this time did not show a recovery. The sample is irreversibly degraded. However, the previously discussed degradation after fabrication (Fig. 5.26) may play an equally high role as the stress measurements.

5.3 Comparison of ZnO-MESFET with competing technologies

With the introduction of MESFET in the oxide-based material system as alternative technology, it has to be compared on the one hand with the established technology of oxide-based MISFET and on the other hand with MESFET devices based on other materials such as GaAs, GaN, etc.

There exist only a few other reports about MESFET based on ZnO. Their difficulties lie in the fabrication of high-quality Schottky contacts. Ryu *et al.* reported MESFET on *p*-type ZnO using Ni as Ohmic and Ti as Schottky contacts, respectively [Ryu05]. Their output characteristics show, that pinch off and saturation are barely obtained for large source-drain voltages in the range of 10 V before breakdown. The gate voltage had to be as large as 20 V to switch the MESFET over a current range of only 1 mA. On the other hand, Kandasamy *et al.* reported a ZnO MESFET for hydrogen gas-sensing applications using Pt Schottky contacts on *n*-ZnO [Kan07a]. However, the saturation current had a strong positive slope, which does not correspond to ideal MESFET characteristics. Kao *et al.* reported a ZnO MESFET using Pt/Au Schottky contacts as gate [Kao05]. Their MESFET also did not show a clear pinch off and saturation. The source-drain current could only be modulated by 4 mA within a gate voltage range of 4 V. Further electrical details such as channel mobility, on/off-ratio etc. were not reported. The Schottky barrier height of Pt was lower (~ 0.68 V) than reported in this thesis (~ 0.9 V), which results in leakage currents larger than 10^{-6} A at −1 V.

MESFET and related logic devices have been also demonstrated on the basis of ZnO nanorods [Par05]. They used metal-organic vapor-phase epitaxially (MOVPE) grown single-

crystalline ZnO nanorods dispersed on SiO_2 and Au-Schottky-contacts using electron-beam lithography to fabricate MESFET as well as OR, AND, NOT, and NOR-gates. The nanorod MESFET exhibit a gate-width-normalized transconductance of 20 μS/μm (compared to 4590 μS/μm for S3 in Fig. 5.5) and a minimal slope between 100 and 200 mV/decade (compared to 80 mV/decade).

The MESFET technology is originated from GaAs devices and intended for the design of high-speed integrated circuits due to its large electron mobility [Miz80, Tuy74]. Therefore, most effort is made in the investigation of this material system. GaAs-MESFET exhibit high channel mobilities of $\sim 3500\,\mathrm{cm^2/Vs}$ compared to the ZnO-MESFET presented in this thesis. Their operation voltage range of $\Delta V_G \sim 1.6\,\mathrm{V}$, turn-on-voltage of $\sim -1\,\mathrm{V}$ [Fol86], and on-off-ratio in the range of $> 10^7$ is comparable to ZnO-MESFET. MESFET have also been developed on the basis of wide-band-gap semiconductors such as GaN, SiC and diamond [Bun07]. Due to the large band gap, high-temperature and high-current stability, those devices are intended for high-power and high-speed applications. The operation voltages for these MESFET are usually higher (in the range of several 10 V up to 100 V) compared to ZnO-MESFET, on/off-ratios and channel mobilities are not considered as important figures of merit. However, e.g. GaN-MESFET have been reported with turn-on-voltages between 11 V and 18 V, having an on/off-ratio in the range of 10^3 and channel mobilities up to $18\,\mathrm{cm^2/Vs}$ [Yos98, Bin97].

Comparing the ZnO MESFET presented in this thesis to the ZnO MISFET in Sec. 4.3 and other reported ZnO-MISFET shows the advantages of MESFET technology (Tab. 5.12). For MISFET, there is often a tradeoff between applied voltage range, on/off-ratio and channel mobility. All MISFET exhibit larger, partially much larger gate voltage ranges in which they achieve the given on/off-ratio. The lowest ΔV_G exhibits the topgate (TG) MISFET presented in this thesis (see Fig. 4.11) with $\Delta V_G = 7\,\mathrm{V}$. However, its channel mobility of $1.9\,\mathrm{cm^2/Vs}$ is rather low compared to the other MISFET in Tab. 5.12. Other ZnO-based MISFET exhibit large channel mobilities of $62\,\mathrm{cm^2/Vs}$ [Sas06] or $40\,\mathrm{cm^2/Vs}$ [Nis05], but their on/off-ratio is only 10^3 or 10^5, respectively. The best relation between voltage range, on-off-ratio and mobility has the single-crystalline indium gallium zinc oxide (IGZO) MISFET of Nomura *et al.* [Nom03]. However, its fabrication on single-crystalline yttria-stabilized zirconia (YSZ) including a 1400°C thermal annealing step after channel growth, is rather complex compared to MESFET.

The MESFET on glass substrates are intended to substitute thin-film transistors made of amorphous silicon in display applications such as active-matrix liquid-crystal (AMLCD) or organic light-emitting-diode (AMOLED) displays. The device parameters of various transistors on glass substrates are compared in Tab. 5.3, where the MISFET consisting of ZTO, GIZO, IZO and AZTO are amorphous. Many of the oxide MISFET as well as the ZnO-MESFET fulfill the requirement of having a channel mobility larger than $1\,\mathrm{cm^2/Vs}$ [Wag03]. However, the reported MISFET channels exhibit larger mobilities and larger on/off-ratios due to higher on-currents. A reasonable source-drain current to be compared with the ZnO MESFET is given by $I = I_0 \cdot \mu/\mu_0$, with I_0 being the maximum current of 1.6 μA and μ_0 the channel mobility of $1.3\,\mathrm{cm^2/Vs}$ of the best ZnO MESFET on glass in this thesis. For example, the gate-voltage range necessary to switch from the off-current $\sim 10^{-11}$ A to I is about $\Delta V_G = 3\,\mathrm{V}$ in [Gö09] and [Cho09] and $\Delta V_G = 4.5\,\mathrm{V}$ in [Lee09c]. The MESFET on glass thus offers a lower operating voltage $\Delta V_G = 1\,\mathrm{V}$. It can be seen from Tab. 5.3, that amorphous-channel MISFET tend to have higher turn-on voltages near $V_T = 0\,\mathrm{V}$, higher on/off-ratios up to 10^{10} [Lee09b] and higher channel mobilities up to $30\,\mathrm{cm^2/Vs}$ [Lee09c] than the ZnO-channel MISFET. Nevertheless,

Table 5.12: Comparison of device parameters for MESFET and MISFET based on oxide channels.

channel	type	ΔV_G (V)	V_T (V)	V_{SD} (V)	on/off	μ_{ch} (cm^2/Vs)	S_{min} (mV/dec)	ref.
ZnO	TG-MESFET	2.4	−1.4	4	1.3×10^8	11.3	81	this work
ZnO	TG-MESFET	1	0	2	2.7×10^6	25	77	this work
ZnO	TG-MISFET	7	−6	4	1.5×10^5	1.9	300	this work
ZnO	BG-MISFET	98	−38	60	6×10^7	0.5	3595	this work
p-ZnO	MESFET	40	2.5	−10	~ 10	–	–	[Ryu05]
ZnO	MESFET	–	–	6	–	–	–	[Kan07a]
ZnO	MESFET	5	< −5	2	< 10	–	–	[Kao05]
IGZO	TG-MISFET	10	0	10	10^6	80	400	[Nom03]
ZnO	BG-MISFET	1975	−975	500	$< 10^7$	68	–	[Suz04]
ZnO	TG-MISFET	13	−13	20	$< 10^5$	40	–	[Nis05]
ZnO	TG-MISFET	> 15	< −10	10	~ 10	5.3	–	[Kao05]
ZnO-QW	TG-MISFET	13	−7	10	10^3	140	770	[Koi05]
ZnO	BG-MISFET	15	−7.2	5	$< 10^3$	62	–	[Sas06]
ZnO	TG-MISFET	37	−32	10	10^8	35	940	[Zhu08]
ZnO	TG-MISFET	30	−15	0.3	$< 10^4$	12	–	[Bel08]

ZnO-MESFET technology is a promising alternative for the fabrication of low-cost electronics for display applications.

Table 5.13: Comparison of device parameters for various transistors on glass substrates. Channel materials: ZTO: zinc tin oxide, GIZO: gallium indium zinc oxide, IZO: indium zinc oxide, AZTO: aluminium zinc tin oxide.

channel	type	ΔV_G (V)	V_T (V)	V_{SD} (V)	on/off	μ_{ch} (cm^2/Vs)	S_{min} (mV/dec)	ref.
ZnO	TG-MESFET	1	0	2	4.7×10^5	1.3	125	this work
ZTO	BG-MISFET	8	−4	10	10^7	5.0	300	[Gö09]
Si:H	BG-MISFET	20	0	20	5×10^5	0.39	494	[Lee09a]
Si:H	BG-MISFET	20	1	16	10^7	0.59	520	[Hua08]
ZnO	BG-MISFET	52	−12	40	10^7	0.4	–	[Hof03]
ZnO	BG-MISFET	10	0	5	10^5	0.03	–	[Mas03]
ZnO	BG-MISFET	25	15	20	2×10^5	20	1240	[For05]
ZnO	BG-MISFET	15	0	10	10^5	1.7	–	[Nav06]
ZnO	BG-MISFET	10	−5	10	10^7	8.4	950	[Hsi06]
ZnO	BG-MISFET	25	15	40	9×10^5	8	900	[Bar06]
ZnO	TG-MISFET	50	−10	40	5×10^7	11	–	[Che07]
ZnO	BG-MISFET	8	< −1	7	1.2×10^3	0.75	1270	[Oh07]
ZnO	TG-MISFET	80	< −40	40	10^4	0.36	–	[Noh07]
ZnO	BG-MISFET	20	−1	20	$> 10^8$	12.9	–	[Lev08]
ZnO	TG-MISFET	30	−5	20	10^7	4.3	500	[Par09]
GIZO	BG-MISFET	3.6	0.4	3	7×10^7	3.3	180	[Cho09]
GIZO	BG-MISFET	11.5	−1.5	10	10^8	30	190	[Lee09c]
GIZO	TG-MISFET	6	0	6	10^8	12	200	[Yab06]
IZO	BG-MISFET	20	−5	10	10^6	0.53	2200	[Son07]
GIZO	BG-MISFET	20	0	10	5×10^7	11	200	[Sur07]
AZTO	BG-MISFET	25	1	10	$> 10^9$	10.1	580	[Cho08]
GIZO	BG-MISFET	30	0	7	5×10^4	0.03	1500	[Kim09a]
GIZO	BG-MISFET	30	0	10	$> 10^7$	14	200	[Sur09]
GIZO	BG-MISFET	20	0	20	10^9	9.5	130	[Sat09]
GIZO	TG-MISFET	20	−1	15	10^{10}	12.2	200	[Lee09b]

6 Inverter

In this chapter, integrated circuits, first and foremost, inverters based on ZnO-MESFET technology are presented. For that, MESFET with ZnO or MgZnO channels on sapphire and Ag_xO-gate contacts were used, since they have shown the best electrically properties and reliability (cf. Sec. 5.1). First, the inverting function will be investigated by means of simple inverters consisting of two MESFET. Figures of merit, such as uncertainty level and peak gain magnitude will be discussed and the observed real voltage-transfer curves are compared to the ideal ones described in Sec. 2.4. Then, properties of inverters with an additional level shifter intended to enable the inverters to be connected in series, i.e. the FET-logic inverter and the Schottky-diode FET-logic inverter, will be presented. The design and measurement of inverters was done in collaboration with F. Schein (Universität Leipzig). Most of the results presented in this chapter were obtained within the scope of his diploma thesis [Sch09]. The analysis of the raw data was done using a script for *OriginPro 8G* written by T. Diez (Universität Leipzig). Measurement software, written by F. Klüpfel (Universität Leipzig), was used for the waferprober automation.

6.1 Simple Inverter

Figure 6.1 shows an optical microscopic image of a simple MESFET inverter fabricated as described in Sec. 3.3. Overlying is the simple inverter circuit (cf. Fig. 2.9a). The load transistor (Q_L, top) and the switching transistor (Q_S, bottom) use a common MgZnO channel layer. Both MESFET have equal gate width-to-length-ratios of $W/L = 430\,\mu m/20\,\mu m = 21.5$ and a gate-source/drain distance of 5 µm.

A typical voltage-transfer curve of a simple inverter and its derivative to determine the *pgm* is depicted in Fig. 6.2. Here, the VTC is obtained for $V_{DD} = 2\,V$. It shows a clear inverting behavior. For negative $V_{in} = -1\,V$, the output high level $V_{OH} = 1.999\,V$ deviates from the ideal case $V_{OH} = V_{DD} = 2V$ only by 1 mV. On the other hand, the output low level $V_{OL} = 0.111\,V$ is achieved for $V_{in} = +0.78\,V$. The ideal value $V_{OL} = 0\,V$ can only be achieved for infinitely steep output characteristics of Q_S (cf. Sec. 2.4.2). Towards $V_{in} = +1\,V$, V_{out} is increasing again, which will be discussed in Sec. 6.1.1. The switching point of this inverter is at $V_{rev} = 0.015\,V$, which is close to the theoretical value of $V_{in} = 0\,V$. The uncertainty level $V_{uc} = 0.325\,V$ is only a factor of three higher than for the GaAs MESFET technology ($V_{uc} \sim 0.1\,V$ [Sed04]).

The *pgm* was determined from the VTC (measured with 5 mV steps) by interpolating the steepest part with a cubic spline and numerical differentiation. Note, that differentiating the raw VTC data would drastically underestimate the gain for inverters with higher gain and lead to a value, which is not comparable to literature since it would depend on the voltage interval used during the measurement. It was ensured in any case, that the *pgm* value approaches its true value and saturates with increasing interpolation point numbers. For the inverter in Fig. 6.2, the *pgm* at $V_{DD} = 2\,V$ was obtained to be

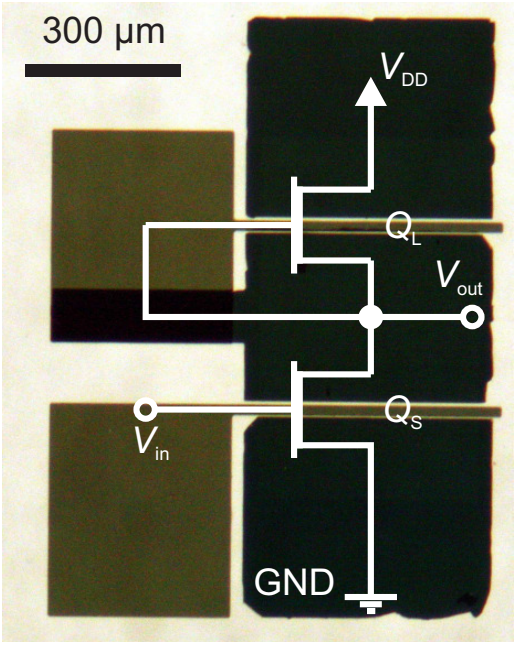


Figure 6.1: Optical microscopic image of the simple MESFET inverter with overlying circuit.

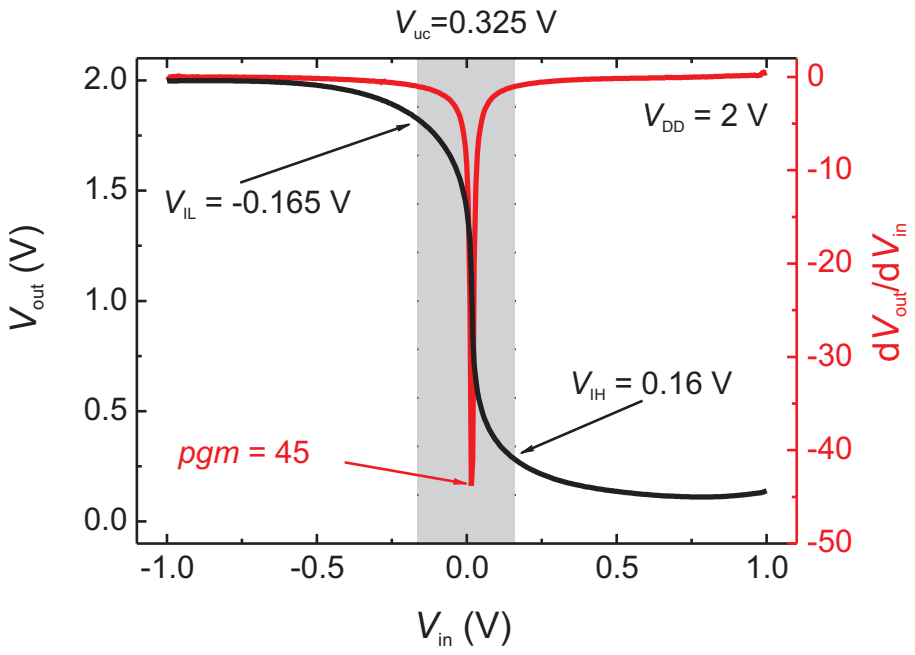


Figure 6.2: Typical voltage-transfer curve and its derivative for a simple MESFET inverter obtained at V_{DD} = 2 V.

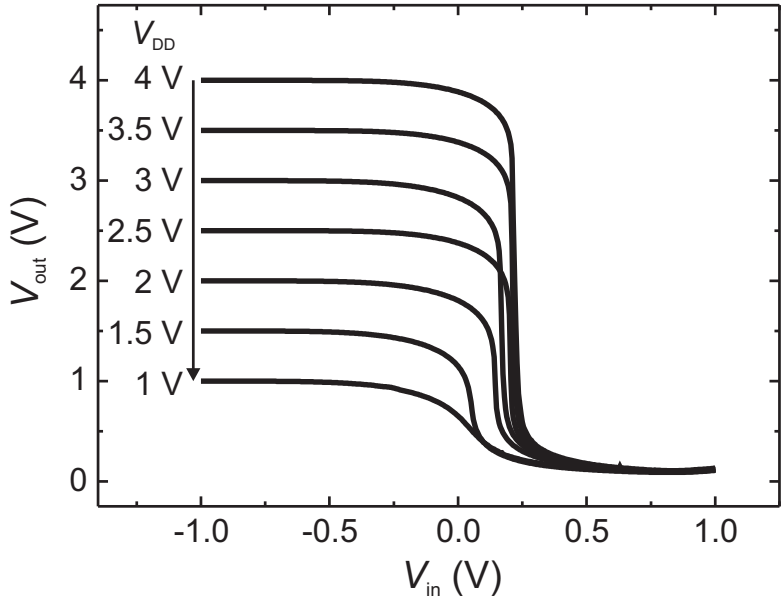


Figure 6.3: VTC of a simple ZnO MESFET-inverter for various V_{DD}.

pgm = 45.

Figure 6.3 shows a set of VTC for various operation voltages V_{DD}. Obviously, V_{DD} determines the high output level V_{OH}. For all V_{DD} between 1 V and 4 V, the respective V_{OH} is reached, whereas the output low level V_{OL} is independent of V_{DD}. The inverting behavior is also preserved for lower operating voltages. However, a shift of the switching point towards positive V_{DD} is observed between V_{DD} = 1.5 V and V_{DD} = 2 V.

It can be seen from Fig. 6.3 that the VTC becomes steeper for higher V_{DD}. The dependence of the pgm and V_{uc} on V_{DD} is depicted in Fig. 6.4. For that, the mean values from 25 inverters on one sample chip were determined; the error bars denote the standard deviation of this statistic. Altogether, 49 inverters are on the mask (see Appendix A). Due to the alignment mask, 13 inverters are covered, 36 inverters remain. As can be seen in Fig. 6.4a, pgm is strongly dependend on V_{DD}. It monotonically increases from pgm = 2.5 for V_{DD} = 1 V to a maximum value of pgm = 170 for V_{DD} = 4 V. It is noticable, that individual inverters reached a maximum gain of pgm = 250 for V_{DD} = 4 V. The mean uncertainty level V_{uc} stays in a voltage range between V_{uc} = 0.3 V and V_{uc} = 0.34 V (Fig. 6.4b). It is smaller for lower V_{DD}, because the variation of V_{in} leads to a smaller deviation of V_{IL} and V_{IH} for lower V_{DD} due to the lower steepness of the VTC. The increasing standard deviation for higher V_{DD} is, on the one hand, due to a stronger statistical spread among the inverters. On the other hand, this is due to the numerical determination of the values; i.e. the measurement points are more apart with respect to V_{out} for steeper VTC.

6.1.1 Real inverter characteristics

The deviations from the ideal VTC of inverters (cf. Sec. 2.4.2) is discussed in this section. Figure 6.5 depicts a VTC, where all three types of deviations can be seen: a) the low-output deviation, where

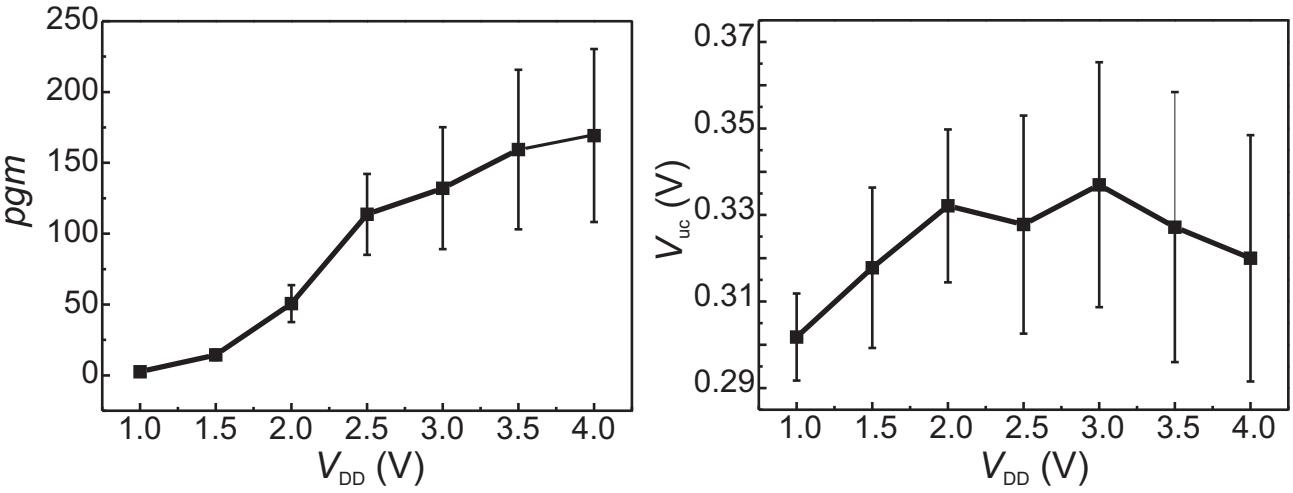


Figure 6.4: a) *pgm* and b) V_{uc} in dependence of V_{DD} (mean values for 25 inverters on one sample chip).

V_{out} starts to increase again after passing through V_{OL}, b) the high-output deviation, where V_{OH} is not achieving V_{DD} and c) the switching-point deviation, where a shift of the switching point towards positive V_{in} occurs.

a) Low-output deviation

The increase of V_{out} for increasing positive V_{in} after the low-output level V_{OL} is due to excessive gate-currents of the MESFET Q_S. As described in Sec. 5, those gate-currents lead to a shift of the output characteristic towards higher V_{SD}. This can also be seen in the simulation depicted in Fig. 6.6a. The shift results in a different position of the intersections with the output curve of Q_L yielding to a higher output voltage as depicted in Fig. 6.6b.

The simulation can be approved considering the currents that flow during the inverter measurement. Such measurement is depicted in Fig. 6.7. I_{in} and I_{DD} denote the current that flows over the gate of Q_S and the source-drain current of Q_L, respectively. It can be seen, that V_{out} of the VTC starts to inrease at $V_{in} \sim 0.7\,\mathrm{V}$, where I_{in} exceeds I_{DD}. Furthermore, the switching point of the inverter is consistent with the point, from whereon I_{DD} is constant and equals the load transistor's saturation current $I_{SD,L}$. At this point $I_{SD,L} = I_{SD,S}$ and for voltages lower than the switching point, it is $I_{DD} = I_{SD,S}$; i.e. the curve $I_{DD}(V_{in})$ is consistent with the switching transistor's transfer characteristic for $V_{in} < V_{rev}$.

b) High-output deviation

The decrease of the VTC for negative V_{in} in the high-output regime of the inverter can be explained by the breakdown of the switching transistor. It occurs for high source-drain voltages, which equal the operation voltage V_{DD}. The higher V_G (in negative direction) and V_{SD} leads to a higher probability of (irreversible) breakdown. This can be seen in the simulation (Fig. 6.8a,b). The intersection point of the output characteristics of Q_S and Q_L for the lowest $V_{G,S}$ occurs at a source-drain voltage of Q_S, which is significantly lower than V_{DD}. Hence, the corresponding point in the VTC is lower, too.

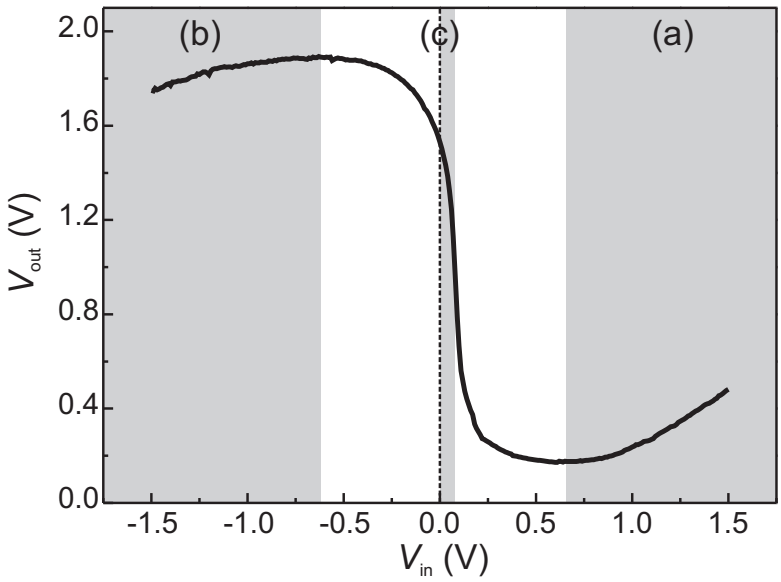


Figure 6.5: Real-inverter VTC with the three types of deviations from the ideal case. a) Low-output deviation, b) High-output deviation and c) Switching-point deviation.

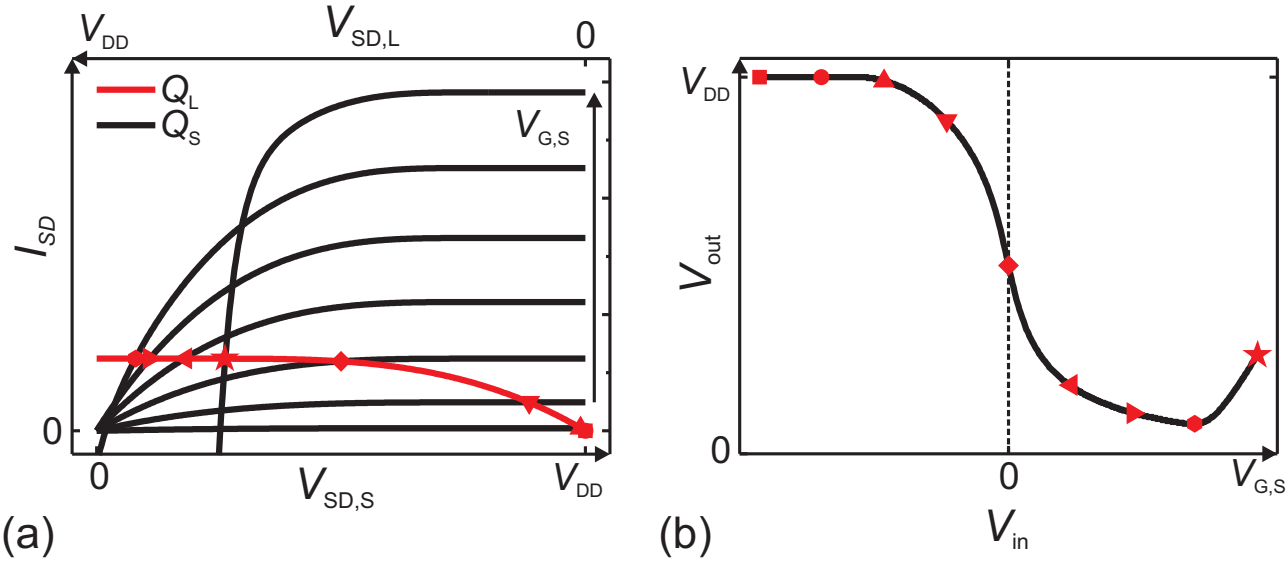


Figure 6.6: a) Simulated output characteristics of the simple inverter's MESFET Q_L and Q_S, where Q_S suffers from excessive gate leakage currents. b) Corresponding VTC with the deviation in the low-output regime.

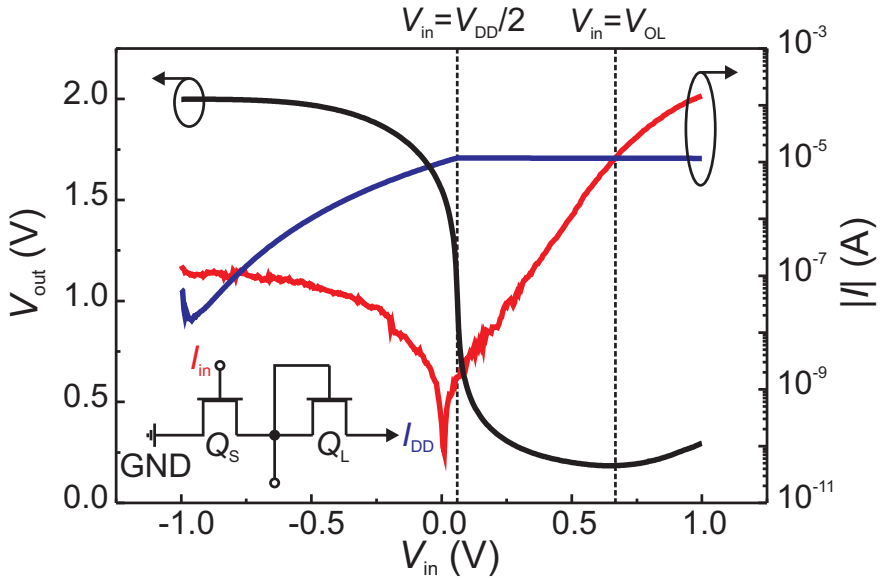


Figure 6.7: VTC and corresponding currents I_{in} and I_{DD} of a simple MESFET inverter at $V_{DD} = 2\,V$. The shifting point and lowest output level are marked with dashed lines.

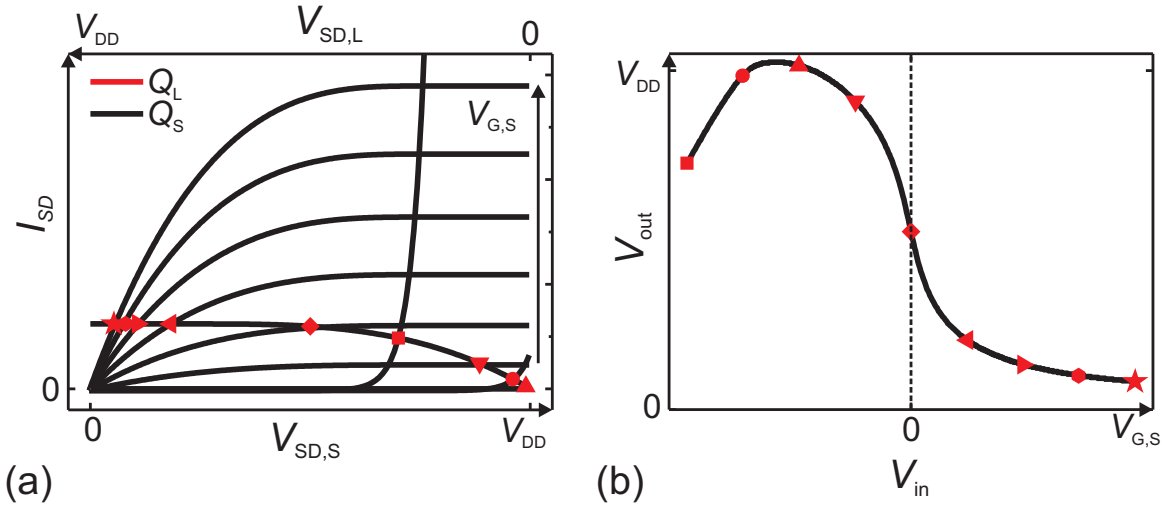


Figure 6.8: a) Simulated output characteristics of the simple inverter's MESFET Q_L and Q_S, where a breakdown occurs for Q_S. b) Corresponding VTC with the deviation in the high-output regime.

A VTC with high-output deviation can be seen in Fig. 6.9b. Figure 6.9a depicts the independently measured output characteristics of Q_S and Q_L. As can be seen from the intersection points marked with symbols, the breakdown that occurs for high negative $V_{G,S}$ is consistent with the deviation in high-output regime of the inverter. It can further be seen, that the output characteristics shift in the linear regime, which leads to a small increase of V_{out} for high V_{in} (low-output deviation) as described in the previous section. From the output characteristics in Fig. 6.9a, the switching point of the inverter is expected to be between $V_{in} = 0\,V$ and $V_{in} = 0.1\,V$. However, the measured switching point in the inverter's VTC is at $V_{rev} = 0.19\,V$. This is probably due to altered voltage relations comparing the

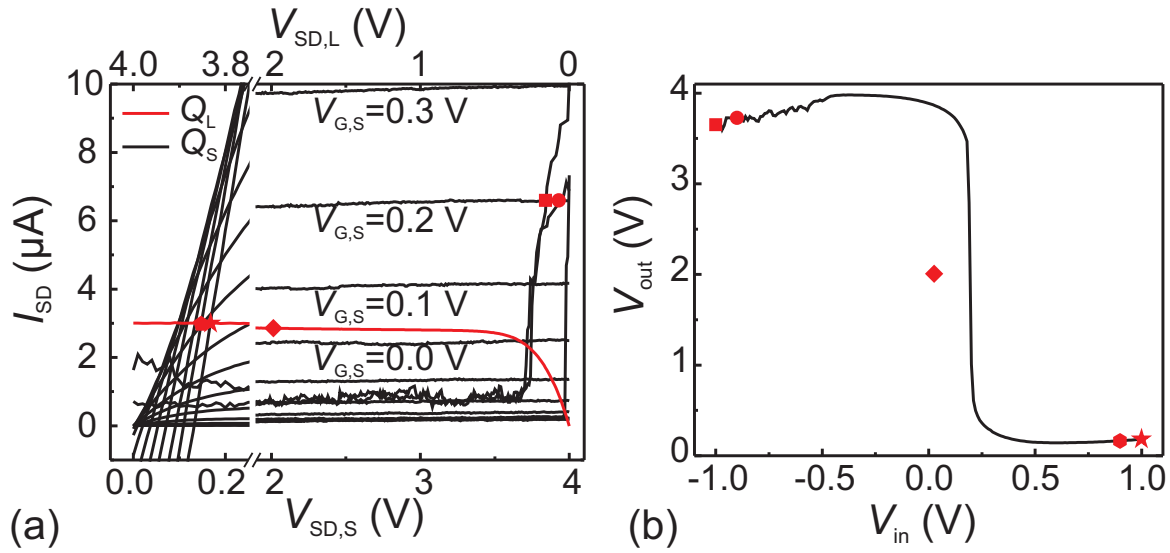


Figure 6.9: a) Individually measured output characteristics of the simple inverter's MESFET Q_L and Q_S with a breakdown occuring for Q_S. b) Corresponding measured VTC of the inverter with high-output deviation.

individually measured MESFET and the interconnected inverter.

c) Switching-point deviation

Due to the equal transistors Q_S and Q_L, the ideal switching point of the inverter is at $V_{rev} = 0\,V$ and $V_{out} = V_{DD}/2$. However, for all inverters measured within this thesis, the input voltage of the switching point is $V_{in} > 0\,V$. This cannot be explained by a variation of the transistor properties, because this would result in a statistically distributed input voltage. In fact, the positive switching voltage can be explained by a higher saturation current at Q_L compared to Q_S, such that higher input voltages have to be applied to level out the transistor's conductivities. This effect can be due to contact resistances or parasitic capacitances. Time and voltage dependent measurements [Sch09] suggest, that a trapping of charge carriers occurs at the Ag_xO-gate of Q_S for positive V_{in}. This correlates with the observation of F. Klüpfel (Universität Leipzig) within his diploma thesis [Klü09], where he compared simple inverters with Ag_xO-gates and with Au-gates. Since the reactively sputtered Au does not form an oxide (Sec. 3.2), for Au-gate inverters, the switching point was always at $V_{rev} = 0\,V$. Furthermore, F: Klüpfel investigated gate-lag and drain-lag effects, i.e. the delayed reaction of the inverters on voltage variations. The Au-gate inverters showed considerably lower reaction times than the Ag_xO-gate inverters, which suggests the presence of less charges at the Au-gates.

6.2 FET-logic Inverter

For the correct operation of a MESFET-inverter based logic circuit, the output of the inverters must not be ambiguous. Therefore, a level-shifter is needed (cf. Sec. 2.4). As a first inverter with level shifter, a FET-logic (FL) inverter shall be considered. An optical microscopic image of the sample

Table 6.1: Summary of deviations in real inverter characteristics.

deviation	reason	possible solution
a) low-output	Shift of the output characteristic of Q_S for low $V_{SD,S}$ and positive $V_{G,S}$ due to leakage gate currents; finite conductivity of the channel	gates with higher Schottky barrier height; higher channel conductivity
b) high-output	breakdown of Q_S for high $V_{SD,S}$ and negative $V_{G,S}$	channel material and Schottky contacts with higher breakdown-field
c) switching-point	parasitic interface charges and capacitances	reduction of the gate interface charges; passivation

with overlying circuit according to Fig. 2.10a is given in Fig. 6.10. The connections for V_{DD}, V_{SS} and GND are designed as lines. This design was chosen because the inverters were intended to be connected in series to form a ring oscillator. Each FL-inverter has five connections: GND, V_{DD}, V_{SS}, V_{in} and V_{out}. The intersection of GND and V_{SS} is designed as insulating cross-over with two additional photolithographic steps. Most suited as insulating layer were the Al_2O_3-ZrO_2-Al_2O_3 sandwich (cf. Cha. 4) and HfO_2 mixed with an amount of Ca as glass moderator with leakage currents of 20 nA at ±3 V. Unfortunately, only 10% of the fabricated FL-inverters are working. For that reason, it was impossible to connect 3 or more inverters in series as ring oscillator. However, as Fig. 6.11a shows, the working FL-inverter proved the principle of level-shiftig as described in Sec. 2.4.2.

Note, that both FL-inverters reach negative low output level $V_{OL} < 0$ V, which would be necessary to securely switch a subsequent inverter connected in series. However, the level-shift of approximately 0.2 V is too small since the uncertainty levels of the inverters are in that voltage range, too. The range between high and low-level is only $\sim$ 1.2 V, contrary to the simple inverters, where it was usually in the range of $V_{DD} - V_{OL}$. V_{OH} is shifted, as expected, by approximately the built-in voltage of two Schottky-diodes. V_{OL}, on the other hand, is increased due to exceeding gate leakage currents.

One reason for the non-ideal characteristics is the insufficient insulating cross-over between V_{SS} and GND. Furthermore, the processing of the insulator, i.e. lift-off of holes for the interconnections, did not work well in any case. Often, insulator material remained at positions were a connection should have been, leading to undesired capacitances which result in large hysteresis effects ($\Delta V \sim 0.15$ V). As Fig. 6.11b shows, high off-currents due to breakdown of Q_S lead to a strong deviation from the ideal VTC in the high-level range (cf. Fig. 6.8). This is probably due to the additionally needed photolithographic steps after deposition of the gate. With that, the samples spent additional time in the oven at elevated temperatures ($\sim$ 90°C), which lead to a degradation of the gate contacts as described in Sec. 5.1. For these reasons, FL-inverters without insulating cross-over were fabricated by means of multiple exposition of the photolithographic masks before and after the step intended for the insulator. Only four instead of six photolithographic steps are needed, similar to the simple inverters. The short-circuited V_{SS} and GND lines are disconnected by scratching with a needle at the respective position (Fig. 6.10). This inhibits the fabrication of ring oscillators.

The results for this FL-inverter are given in Fig. 6.12 as a function of V_{DD} (Fig. 6.12a,c,e) and V_{SS} (Fig. 6.12b,d,f). The VTC is shifted towards negative V_{out} by approximately 1.2 V, which corresponds to the built-in voltage of two ZnO Schottky diodes connected in series. The hysteresis of the VTC

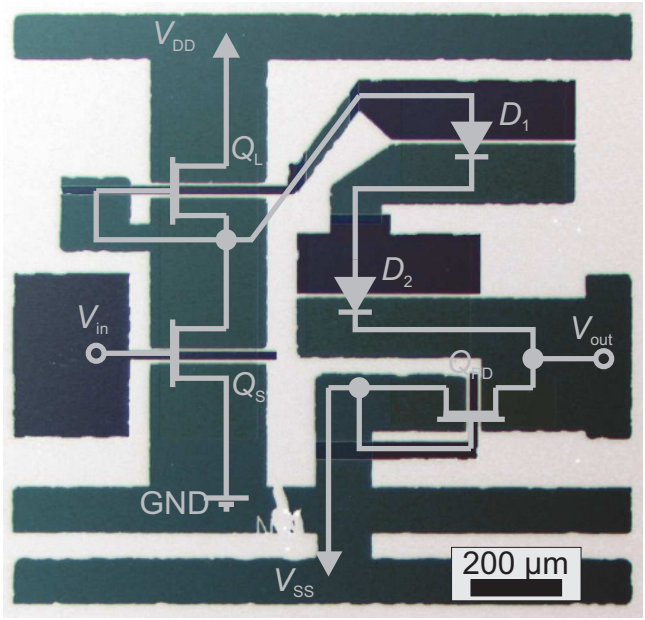


Figure 6.10: Optical microscopic image of an FL-inverter with overlying circuit. The width-to-length ratios of Q_S/Q_L and Q_{PD} are W/L = 210 µm/20 µm and W/L = 105 µm/20 µm, respectively. The GND line is manually disconnected (see text).

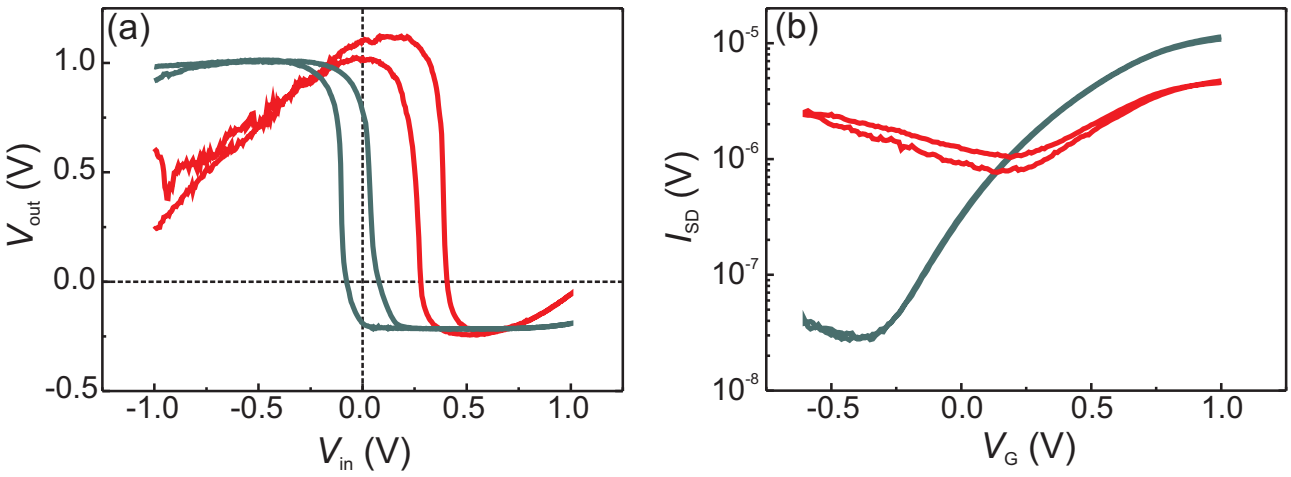


Figure 6.11: a) Best VTC (input-voltage cycling) of working FL-inverter with insulating cross-over at V_{DD} = 2 V and V_{SS} = −1 V. b) Corresponding transfer characteristics of Q_S at V_{SD} = 2 V.

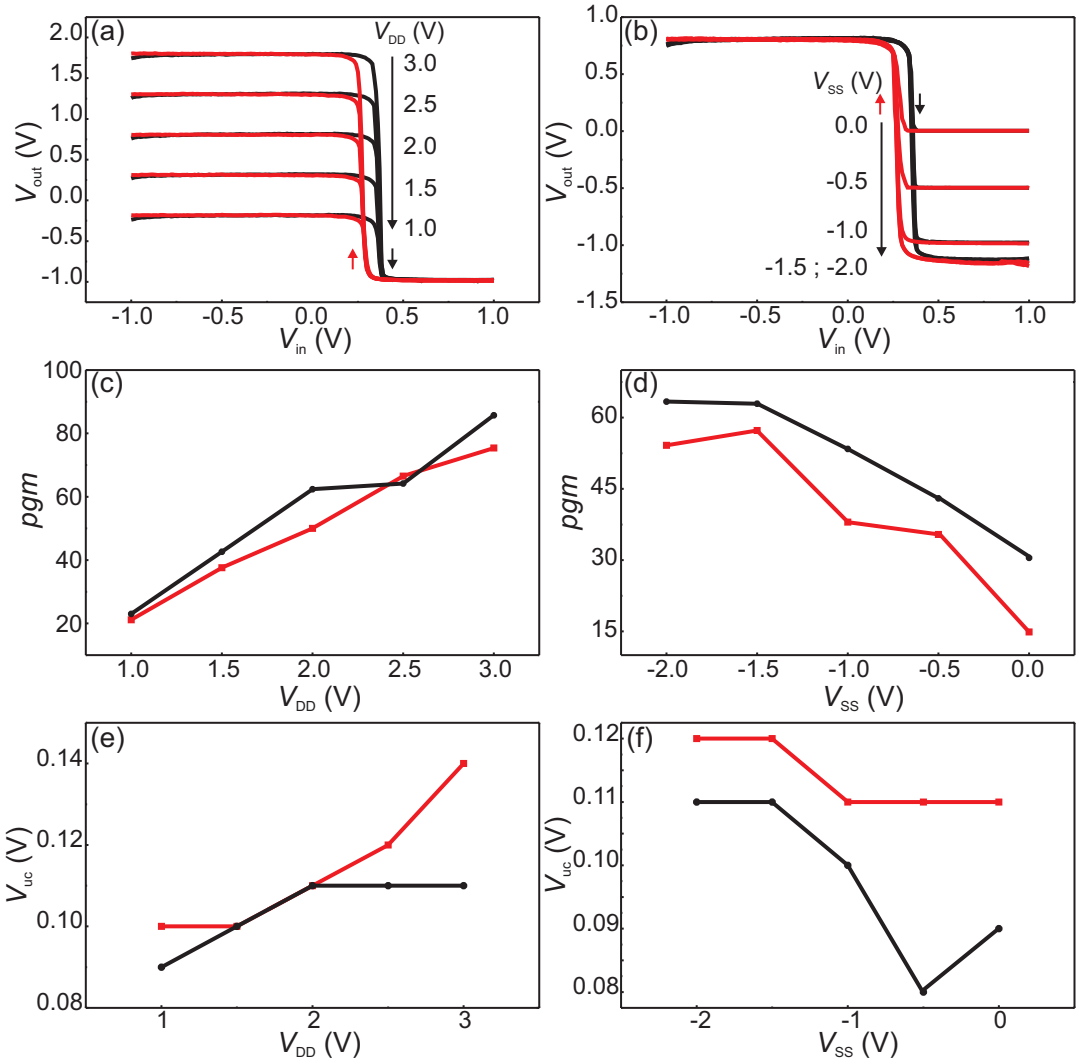


Figure 6.12: Characteristics of an FL-inverter without insulating cross-over (input-voltage cycling). a,c,e) VTC, *pgm* and V_{uc} as function of V_{DD} and b,d,f) as a function of V_{SS}.

$\Delta V \sim 0.09\,\text{V}$ is significantly lower than for the FL-inverter with insulating cross-over. The dependence on the operation voltage of the pull-down transistor V_{SS} shows (Fig. 6.12b) that the level shift is limited to the Schottky diode's built-in voltages. The VTC shift saturates for $V_{SS} = -1.5\,\text{V}$ and $V_{SS} = -2.0\,\text{V}$. This limitation can also be seen in Fig. 6.12d and f, for the *pgm* and V_{uc}. The uncertainty level V_{uc} is very low compared to the FL-inverter with insulating cross-over or compared to the simple inverters in the previous section. It lies in the range between $V_{uc} = 0.08\,\text{V}$ and $V_{uc} = 0.14\,\text{V}$ and is slightly increasing for increasing V_{DD} and negative increasing V_{SS}. The determined *pgm* (Fig. 6.12c,d) is underestimated due to the low V_{uc} which results in less measurement points within the switching range.

Due to the level shifter, it is now possible to obtain logic levels, which are compatible with subsequent normally-on gates. This could be for example $(V_{out}|V_{in}) = (\pm 0.8\,\text{V}| \pm 0.8\,\text{V})$ for $V_{DD} = 2\,\text{V}$ and $V_{SS} = -0.8\,\text{V}$. However, the rate of working FL-inverters still needs to be improved.

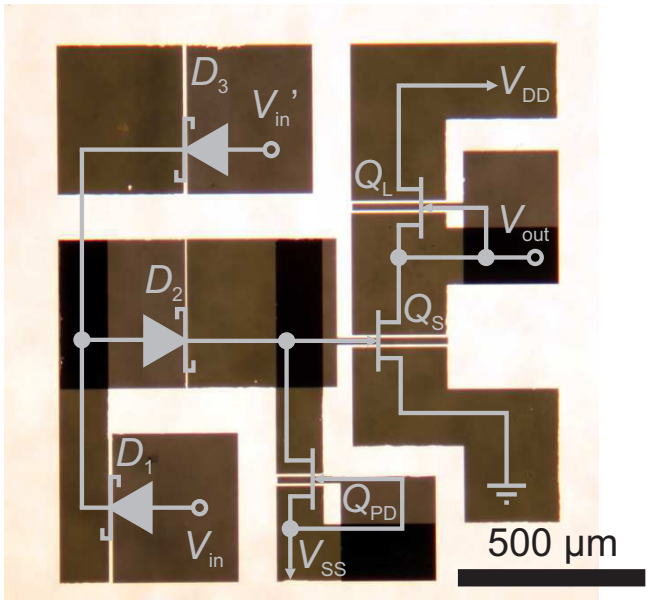


Figure 6.13: Optical microscopic image of the SDFL inverter with overlying circuit.

Table 6.2: Properties of the inverter part (without level shifter) of SDFL inverters with ZnO channel and MgZnO channel (best inverters).

channel	d (nm)	$N_D - N_A$ (10^{17} cm^{-3})	V_T of Q_S (V)	V_{DD} (V)	*pgm*	V_{uc} (V)	yield (%)
MgZnO	21	3.4	−0.25	3	197	0.13	90
ZnO	28	2.5	−1.1	3	141	0.37	60

6.3 Schottky-diode FET-logic Inverter

As a second inverter of the FET-logic family, a Schottky-diode FET-logic inverter is considered [Fre10b]. Figure 6.13 depicts an optical microscopic image of the inverter with overlying circuit according to Fig. 2.11a,b. Here, the level-shifting part consisting of two Schottky diodes D_1 and D_2 is connected at the input side of the fundamental inverting part. This circuit design has the possibility to implement a NOR-gate by manually connecting a third diode D_3 to D_2 using conductive epoxy resin. This will be discussed at the end of this section. This kind of inverter is fully processed using four photolithographic steps (Sec. 3.3). However, due to the contact design, an implementation of a ring oscillator is not yet possible. The SDFL design permits to investigate the properties of the inverter without level shifter (LS), with one-diode LS and with two diodes as LS by connecting the probe tips to the according contact pads.

VTC were measured for two SDFL-inverter samples with a 29 nm thick ZnO channel and a 21 nm thick MgZnO channel. The measured properties are summarized in Tab. 6.2. ZnO and MgZnO are compared because, as described in Sec. 5.1, MgZnO-FETs are more stable, reproducable and reliable than pure ZnO. Both samples were processed equally and exhibit a similar net doping concentration of 3×10^{17} cm^{-3}, obtained from QSCV measurements. In Fig. 6.14, the VTC and transfer charac-

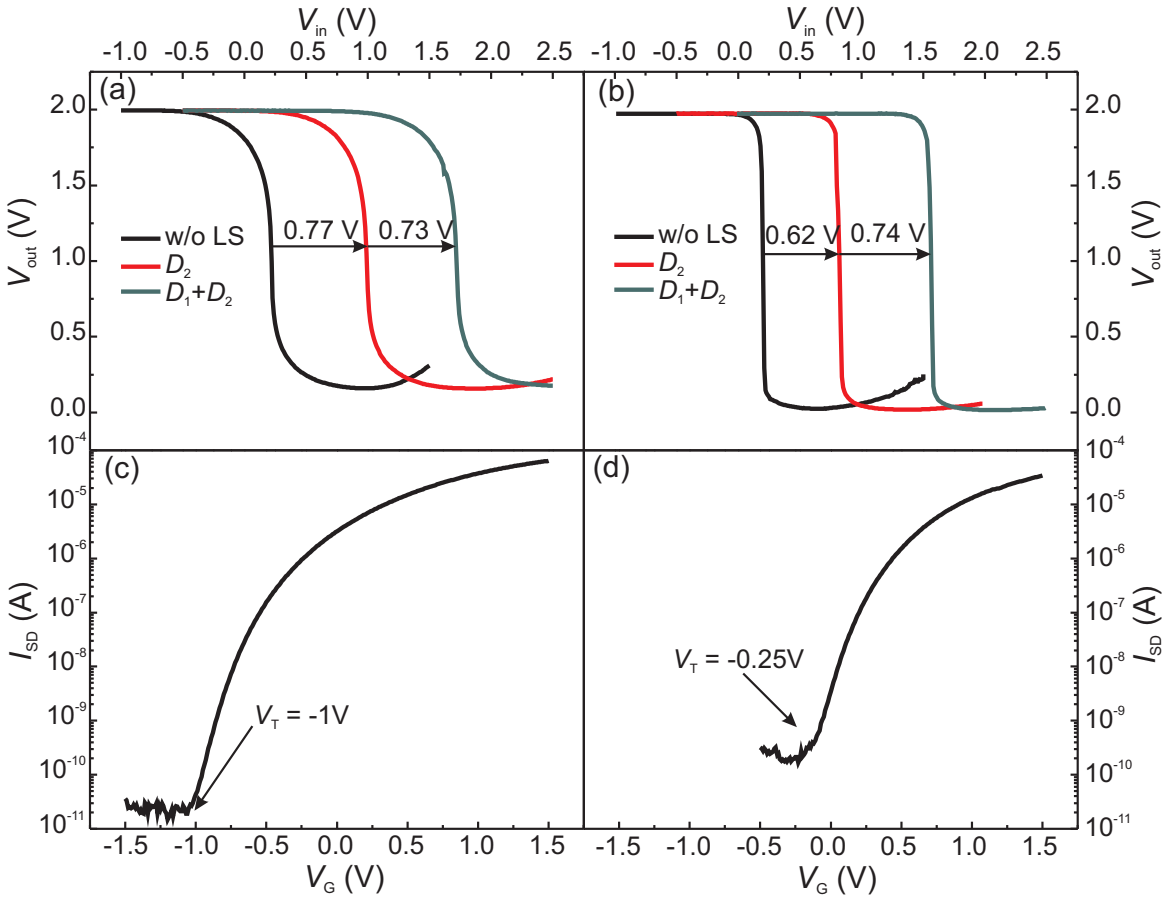


Figure 6.14: a, b) VTC for the SDFL inverters on a) ZnO and b) MgZnO without level shifter (LS), with one diode (D_2) and with two diodes ($D_1 + D_2$) using $V_{SS} = -1$ V. c,d) Corresponding transfer characteristics of the switching transistor Q_S at $V_{SD} = 2$ V.

teristics of Q_S are compared for the SDFL-inverter with ZnO channel and MgZnO channel. The main difference between the two samples is, that Q_S is normally-on ($V_T = -1$ V) for ZnO and nearly normally-off ($V_T = -0.25$ V) for MgZnO. Although the circuit is designed for normally-on MESFET, the performance of the inverters is improved for V_T being closer to 0 V. On the one hand, this is due to the higher currents that flow through normally-on MESFET at $V_G = 0$ V. On the other hand, as already been shown for the MESFET on glass (Sec. 5.2), for more positive V_T, the slope of the transfer characteristic is steeper. For ZnO, this results in VTC which are comparable to the simple inverter (Sec. 6.1) having $V_{OH} = V_{DD} = 2$ V and $V_{OL} \sim 0.16$ V. For MgZnO, the VTC are steeper, also having $V_{OH} = V_{DD} = 2$ V, but a lower $V_{OL} \sim 0.02$ V. The LS shifts the VTC by 0.77 V (0.62 V) for ZnO (MgZnO) using one diode D_2 and by 1.5 V (1.36 V) using two diodes $D_1 + D_2$, according to the voltage drop occuring at the ZnO Schottky diodes. With that, adequate operating points for the two-diode SDFL inverter would be e.g. ($V_{in}|V_{out}$) = (2 V|0 V) and (0 V|2 V). Thus, the output low level of the inverter (logic "0") fits to the subsequent inverter leading to a secure high output level (logic "1"). Choosing $V_{OH} = 2$ V as high level, it is even sufficient to use only one diode for the level shifter. Then, the switching point is at $V_{out} = 0.83$ V, i.e. close to the ideal value of $V_{out} = V_{DD}/2 = 1$ V.

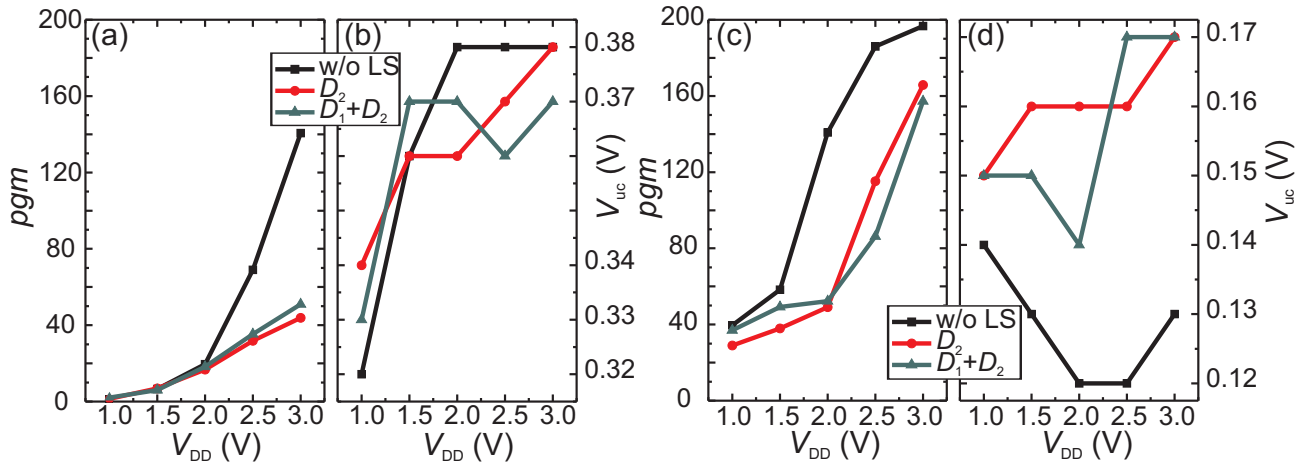


Figure 6.15: a,c) *pgm* and b,d) V_{uc} for the SDFL inverters on a,b) ZnO and c,d) MgZnO without level shifter (LS), with one diode (D_2) and with two diodes (D_1 + D_2) as a function of the supply voltage V_{DD} and with $V_{SS} = -1$ V.

The different threshold voltages of Q_S for the inverter on ZnO and on MgZnO are only determined by the channel thickness, because the net doping concentration lies in the same range (cf. Tab. 6.2). The higher steepness of the MgZnO inverter can be explained by the higher change of $I_{SD,sat}$ of Q_S relative to Q_L for an equal input voltage change $\Delta V_{in} = \Delta V_{G,Q_S}$:

$$\frac{\Delta I_{SD,sat,Q_S}}{I_{SD,sat,Q_L}} = \frac{I_{SD,sat,Q_S}(0.1\,\text{V}) - I_{SD,sat,Q_S}(-0.1\,\text{V})}{I_{SD,sat,Q_L}(0\,\text{V})}\,, \tag{6.1}$$

which is 3.53 for MgZnO and 0.82 for ZnO. The slope S of the transfer characteristic of the MgZnO inverter is higher around $V_G = 0$ V than for the ZnO inverter. In the first case, a smaller ΔV_{in} is adequate to level out the channel conductivities of Q_S and Q_L, which results in a lower uncertainty level and higher peak gain magnitude.

The dependence of V_{uc} and *pgm* on the operating voltage V_{DD} is depicted in Fig. 6.15. For the ZnO inverter without LS, *pgm* (Fig. 6.15a) increases from *pgm* = 1.5 at $V_{DD} = 1$ V to *pgm* = 141 at $V_{DD} = 3$ V. The *pgm* is higher for the MgZnO inverter without LS (Fig. 6.15c), increasing from *pgm* = 40 at $V_{DD} = 1$ V to *pgm* = 197 at $V_{DD} = 3$ V. In both cases, adding the LS leads to lower *pgm* due to additional resistances and leakage currents over the diodes and the pull-down transistor Q_{PD}. V_{uc} for the MgZnO inverter (Fig. 6.15d) stays almost constant for varying V_{DD}. It is slightly higher for the inverter with LS ($V_{uc} = 0.17$ V at $V_{DD} = 3$ V) than for the simple inverter part ($V_{uc} = 0.13$ V at $V_{DD} = 3$ V). This can also be traced back to imperfections of the diodes and Q_{PD}. For the ZnO inverter, V_{uc} was drastically higher than for the MgZnO inverter. It slightly changes from $V_{uc} = 0.33$ V at $V_{DD} = 1$ V to $V_{uc} = 0.37$ V for $V_{DD} > 1$ V, probably due to the effect of a parasitic capacitance at the gate of Q_S.

The here presented VTC were measured for $V_{SS} = -1$ V. However, a variation of V_{SS} between -2 V and 0 V did not show any variation of the VTC. Furthermore, not until $V_{SS} = 0.3$ V, the VTC starts to break down. For $V_{SS} > 0.3$ V, no inverting behavior is observed. It is assumed, that this is due to the

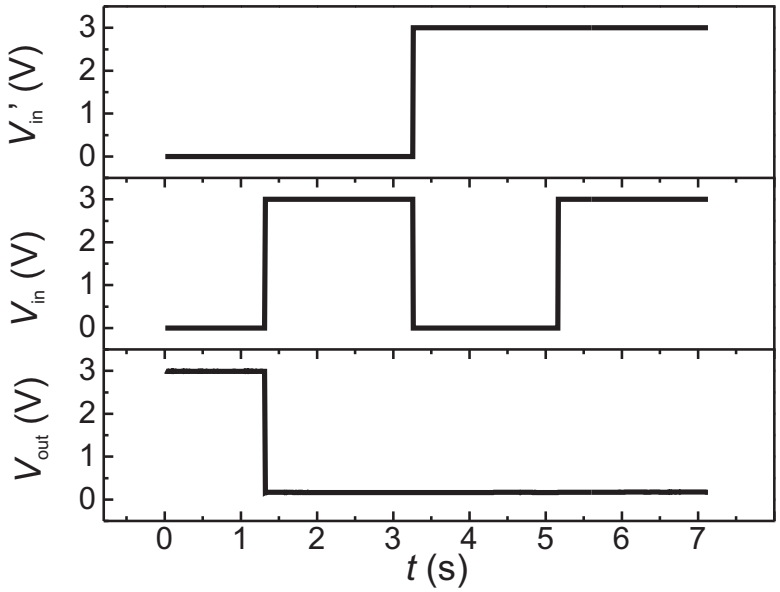


Figure 6.16: NOR-function of a SDFL inverter using D_3 as second input V'_{in}.

effect of trapped charges, which alter the voltage at Q_{PD} such that an external voltage in the magnitude of the switching-point deviation (cf. Sec. 6.1) has to be applied to reach $V_{\mathrm{SS}} = 0\,\mathrm{V}$.

By connecting the third diode D_3 as second input V'_{in} with D_2 (Fig. 6.13), a SDFL NOR-gate is implemented. For that, the connection is realized using a conducting epoxy resin, which had to be annealed at 90°C for one hour in an oven. Using a gold wire, the second input is connected to a metal plate on which the whole sample was mounted. With that, the waferprober's chuck was used as sixth probe.

The measurement of the NOR-function is depicted in Fig. 6.16. The input voltages were applied for seconds. The high output level was chosen to be $V_{\mathrm{OH}} = V_{\mathrm{DD}} = 3\,\mathrm{V}$, such that $(V_{\mathrm{in}}|V_{\mathrm{out}}) = (3\,\mathrm{V}|0\,\mathrm{V})$ and $(0\,\mathrm{V}|3\,\mathrm{V})$. The measurement clearly shows, that the output NOR is only logic "1" (high) if both input levels V_{in} and V'_{in} are logic "0" (low) (cf. Fig. 2.6b). With $V_{\mathrm{OH}} > 2.99\,\mathrm{V}$ and $V_{\mathrm{OL}} < 0.18\,\mathrm{V}$, the two logic levels are very good distinguishable.

6.4 Comparison with MESFET inverter devices from the literature

MESFET-based inverter circuits are commonly known from the GaAs technology. However, they have also been demonstrated on other material systems. In Tab. 6.3, inverter parameters are compared for various materials. It is noticable, that the gain values for the respective inverters are not as high as for the ZnMgO-MESFET inverter, whereas the uncertainty levels are similar. For GaAs and AlGaN/GaN-HEMT inverters, the switching speed (which is determined by means of ring oscillators) is of higher importance. The highest gain of 83 exhibit a simple MESFET inverter consisting of CdS nanowires with In/Au contacts reported by Ma *et al.* in 2007 [Ma07]. One year later, they reported

Table 6.3: Comparison of MESFET inverter parameters.

channel	type	*pgm*	V_{rev} (V)	V_{uc} (V)	V_{DD} (V)	V_{SS} (V)	ref.
$Zn_{0.997}Mg_{0.003}O$	SDFL	197	0.2	0.13	3	−1	this work
GaAs	SDFL	~ 4	~ 1.1	~ 0.5	2.5	−1.2	[Hel82]
GaAs	BFL	~ 6	0	~ 0.29	2.5	−1.5	[Ros91]
AlGaN/GaN	E-D	4.2	~ 1	~ 0.41	2.5	–	[Cai06]
AlGaN/GaN	E-D	4.9	~ 1	~ 0.5	3	–	[Cai07]
diamond	DCFL	1.6	–	–	−2.4	–	[Ito95]
Si	CMES	~ 5	0.2	~ 0.14	0.4	–	[Nyl88]
CdS-NW	SI	83	~ 0.2	~ 0.1	5	–	[Ma07]
n-CdS/p-Zn_3P_2	CMES	20	−0.5	~ 0.1	1	–	[Ma08]

a complementary MESFET (CMES) inverter with *n*-type CdS and *p*-type Zn_3P_2 nanowires with a *pgm* of 20. The complementary technology, which is also reported for Si-MESFET inverters [Nyl88] has the advantage of low power dissipation. The static power dissipation of the CdS/Zn_3P_2-nanowire inverter, normalized with the switching transistor's gate area is $P_D = 85.7\,pW/\mu m^2$ at $V_{DD} = 1\,V$. This is, however, of the same order as the MgZnO-based SDFL inverter presented in this thesis, where at $V_{DD} = 3\,V$ and $V_{SS} = -1\,V$ the low-output power dissipation is $P_D = 111\,pW/\mu m^2$ and for high-output it is $P_D = 46\,pW/\mu m^2$. For the ZnO-SDFL inverter in this thesis, it is $P_D = 476\,pW/\mu m^2$ and $P_D = 5000\,pW/\mu m^2$ for the high and low output, respectively, due to one and two orders of magnitude higher currents through the MESFET. However, these values are still low compared to GaAs inverters (34-45 $\mu W/\mu m^2$ [Ede78a]) or AlGaN/GaN-HEMT inverters (444 $\mu W/\mu m^2$ [Cai07]). A comparison of device parameters of transparent inverters is separately given in Tab. 7.2.

7 Transparent rectifying contacts

The presented MESFET devices in the previous chapters were not transparent. Their source and drain contacts were made of a thick gold layer and the two-layer structure of the gate contact was processed as described in Sec. 3.2. The tremendous advantages of the MESFET technology were demonstrated on these opaque devices. However, the aim is to enable a new approach to transparent electronics and therefore to transfer the shown advantages to transparent MESFET devices. To achieve this, transparent rectifying contacts (TRC) were fabricated on ZnO [Fre09b, Fre10a]. In this chapter, transparent Schottky diodes, MESFET and inverters are demonstrated. The work on TRC is done in collaboration with A. Lajn (Universität Leipzig).

7.1 Preparation

The samples for the three different devices were grown by PLD (Sec. 3.1) on as-received *a*-plane sapphire substrates. Table 7.1 summarizes the individual structure and growth parameters. A 2-inch wafer with a layer sequence of 300 nm degenerately doped ZnO:Al and 800 nm undoped ZnO was contacted in front-to-back geometry to ensure low series resistances [Wen06] for the Schottky diodes. To prepare the MESFET and inverters, two pieces of a 50×50 mm^2 sapphire wafer with a 30 nm thick nominally undoped MgZnO film were used. The thickness of the MgZnO film for the MESFET and inverter was measured by a field-emission microscope (FEM) at a crosssection prepared by a focussed Ga-ion beam, whereas the thickness of the ZnO:Al and ZnO for the Schottky diodes was estimated from the number of pulses and the established nominal growth rate. XRD measurements were performed on the as-grown channel layer of the MESFET and inverters. The *c*-oriented layer showed no shift of the ZnO reflexes and no additional phases due to incorporation of Mg were observed. The FWHM of a corresponding ω-scan (rocking curve) of the ZnO (0002) peak is 1.1°. AFM of the as-grown channel layer shows grains in the size of 30 nm within a homogeneously closed surface and a rms roughness of 0.65 nm determined from a 1×2 µm^2 scan area. These values are in a typical range for such thin ZnO films on sapphire as shown in Sec. 5.2 and in [Fre09c].

The shape of the sputtered TRC investigated as Schottky diodes was defined by molybdenium steel

Table 7.1: Overview of the used structure and PLD parameters for transparent devices.

sample	substrate	layer	p_{O_2} (mbar)	target	freq. (Hz)	d (nm)	T_S (°C)
SD	*a*-Al_2O_3 (2")	ZnO	0.04	ZnO (5N)	25	~ 1000	700
		ZnO:Al		ZnO+1 wt-% Al_2O_3	20	~ 300	
MESFET & Inverter	*a*-Al_2O_3 (50×50 mm^2)	MgZnO	0.02	ZnO+0.25 wt-% MgO	3	30	670

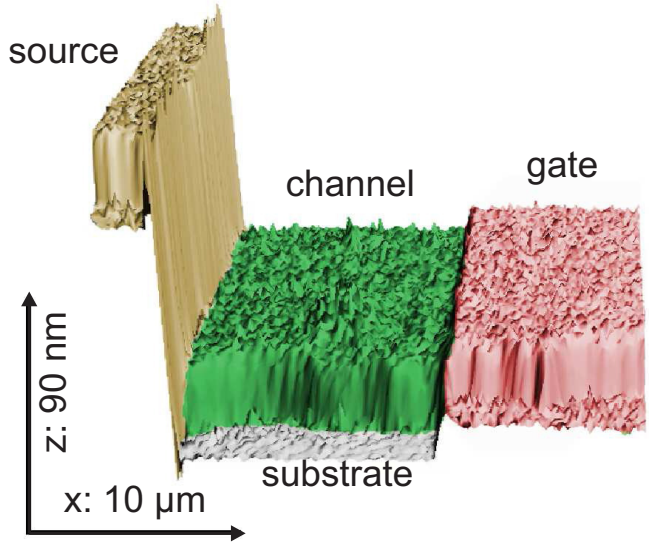


Figure 7.1: AFM picture of the as-processed surface of a transparent MESFET. Source: ZnO:Al, channel: ZnO, gate: Au/Ag_xO, substrate: Al_2O_3. (Measurement performed by M. Lorenz (Universität Leipzig))

shadow masks. The MESFET and inverters were processed using photolithography as described in Sec. 3.3. For the sake of transparent devices, the ohmic source and drain contacts were deposited either by dc sputtering of very thin Au under an Ar atmosphere for the inverters or by growing a highly conducting layer of ZnO doped with 3 wt-% Al by PLD at room temperature and an oxygen partial pressure of 0.016 mbar for the MESFET. The specific contact resistivity of this layer obtained by a transmission line method [Jan06] was in the range of 10^{-4} Ωcm^2. The TRC were fabricated using a modification of the two-step dc sputtering process which was used for the opaque MESFET (Tab. 3.2). First, an ultrathin layer of Ag_xO or PtO_x was reactively sputtered under a mixture of 50% Ar and 50% O_2 for a longer time (30 s) but at lower power (5 W) than the standard parameters (cf. Tab. 3.2). Under these conditions, the thickness of the oxide layer is around 5 nm and the contacts are transparent. Due to the small thickness and oxidation of the first layer, its sheet resistance is rather high. Therefore, a current spreading layer of Au (on Ag_xO) and Pt (on PtO_x), respectively, was sputtered under a pure Ar atmosphere in order to ensure an equipotential surface and therewith reduce the series resistance. This step is even more important for the ultrahin metalloxide layers. The overall thickness of the contact structure is only about 10 nm. Figure 7.1 shows an AFM image of the as-processed device surface in an area between source and gate contact at the edge of the channel mesa. Due to the etching of the mesa structure, the rms roughness of the sapphire substrate and the ZnO channel is rather high (1.9 nm and 1.2 nm, respectively) compared to 0.65 nm of the as-grown channel layer. This, however does not impact the properties of the TRC. It can be seen, that the surface of the transparent gate contact is equally smooth (1.5 nm) and the TRC layer is closed despite of its very small thickness. The source (and drain) contact (ZnO:Al) is 89 nm thick.

The combination of an ultrathin, non-insulating metal-oxide layer with an equally thin conducting capping layer leads to high transparency of the contact under perpetuation of its high rectifying function. In later designs, the metallic capping layer can be substituted with a TCO which would increase the transparency. The mean transmission (Fig. 7.2) of the complete device structure (substrate, ZnO

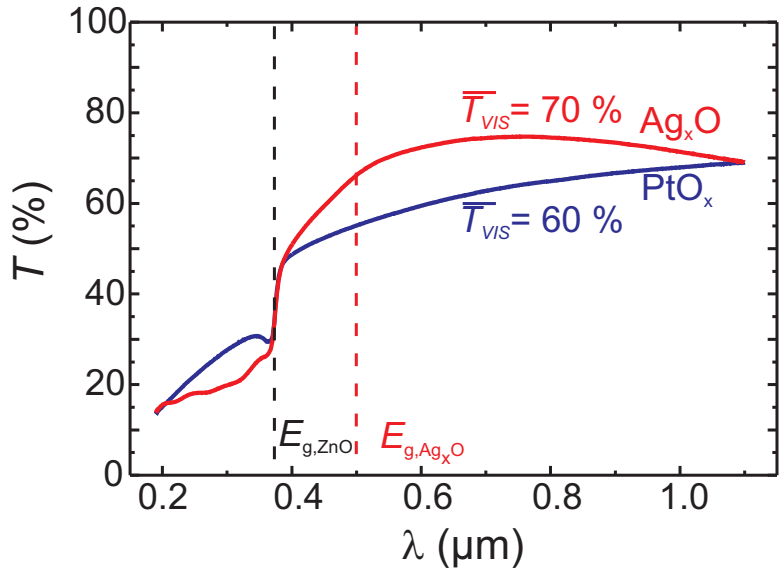


Figure 7.2: Transmission spectra of a complete TRC structure including substrate, channel and contact.

channel and TRC) with Ag_xO and PtO_x as TRC in the visible spectral range (400 nm - 800 nm) is 70% and 60%, respectively. The maximum transmittance for Ag_xO is 74% at 740 nm. However, for the green and blue spectral range, Ag_xO shows a decreasing transmission, which is due to its fundamental absorption edge at (2.5 ± 0.2) eV, which was derived from the onset of the absorption coefficient obtained by spectroscopic ellipsometry measurements performed by Helena Hilmer (Universität Leipzig). Both samples show an absorption edge at 375 nm due to the underlying ZnO layer.

7.2 Transparent Schottky diodes

Figure 7.3 shows the diode characteristics of transparent Ag_xO- and PtO_x-contacts obtained at room temperature and ambient atmosphere. The rectification ratio (not corrected for the series resistance) at ±2 V is 4.8×10^6 for Ag_xO and 1.5×10^6 for PtO_x, respectively. The ideality factors η, series resistances R_S and barrier heights Φ_B were extracted from a fit using the thermionic emission model (Sec. 2.1.3). For Ag_xO (PtO_x), η and Φ_B are 1.47 (1.52) and 0.84 eV (0.87 eV). The higher R_S = 1.7 kΩ for PtO_x compared to Ag_xO (R_S = 0.4 kΩ) is explained by a slightly larger layer thickness. The increase of the reverse currents for both samples is not due to a parallel resistance R_P; instead a laterally inhomogeneous and therefore voltage dependent barrier height is assumed [Wen06].

7.3 Transparent MESFETs

On the basis of the TRC, transparent MESFET were fabricated. An optical microscopic image of the contact structure with PtO_x is given in Fig. 7.4. The source- and drain-contacts were formed by the TCO ZnO:Al and were grown by PLD at room temperature. The mean transmission of the

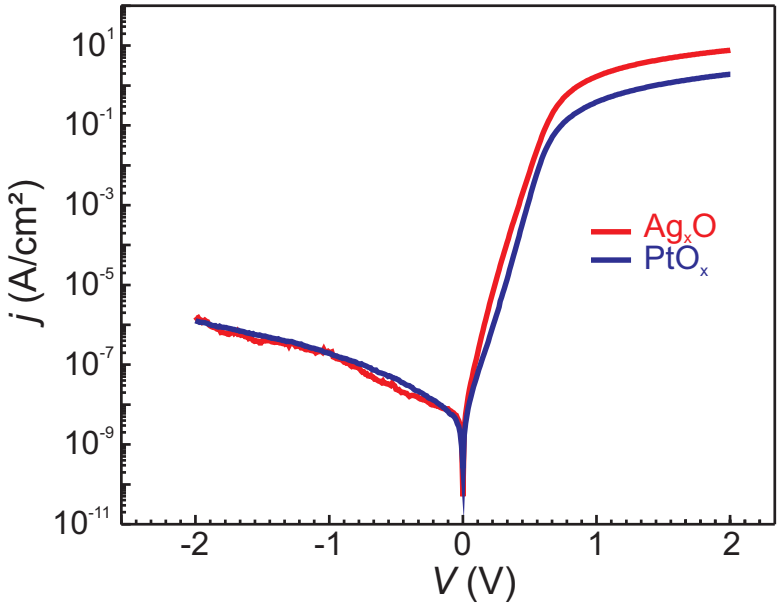


Figure 7.3: Current-voltage measurements of transparent Schottky diodes.

device in the visible spectral range reaches 87% through the source/drain-contacts and 62% through the PtO_x-gate.

A typical output characteristic of a transparent Ag_xO-gate MESFET is depicted in Fig. 7.5a. It shows the clear linear and saturation region within a drain voltage sweep between 0 and 2.5 V and strong dependence on the gate voltage. The curve for $V_G = 1$ V shows a small offset of the source-drain current due to excessive currents over the gate. Figure 7.5b shows transfer characteristics of the same Ag_xO MESFET and a PtO_x-gate MESFET for a source-drain voltage $V_{SD} = 2$ V. These normally-on FETs have on/off-ratios of $I_{on}/I_{off} = 1.3 \times 10^5$ for PtO_x and 1.4×10^6 for Ag_xO and turn-on voltages of $V_T = -1.71$ V and -1.26 V, respectively. The lower negative turn-on voltage for Ag_xO is due to the indiffusion of Ag into the ZnO channel, which serves as compensating defect in the n-type semiconductor [Ahn06a]. The off-currents are limited by the TRC's leakage current and lie in the range of nanoamperes (PtO_x) and 100 picoamperes (Ag_xO). The on-currents reflect the series resistances of the channels and are limited by the forward gate voltage, for which the TRC is in flatband condition. With the channel's width-to-length-ratio $W/L = 10.75$, the channel mobility μ_{ch} is determined from the maximum transconductance g_{max} (Eqn. 2.63). The net doping concentration obtained from QSCV measurements were $N_D - N_A = 3.0 \times 10^{18}$ cm^{-3} for the PtO_x-MESFET and 1.4×10^{18} cm^{-3} for the Ag_xO-MESFET, which is again ascribed to the compensation by Ag. With that the channel mobilities are $\mu_{ch} = 11.4$ cm^2(Vs)$^{-1}$ and $\mu_{ch} = 11.9$ cm^2(Vs)$^{-1}$ for PtO_x and Ag_xO, respectively.

The reproducibility of the devices is demonstrated exemplarily for PtO_x in the histogram (Fig. 7.5c) for all MESFET ($N = 38$) on a cutted 10×10 mm^2 piece of the fabricated wafer. The mean channel mobility is $\overline{\mu_{ch}} = 10.4$ cm^2(Vs)$^{-1}$ with a standard deviation of $\sigma_\mu = 1.1$ cm^2(Vs)$^{-1}$. The median of the logarithmic on/off-ratio is $r = \log_{10}(I_{on}/I_{off}) = 4.9$ with $\sigma_r = 0.5$. The reproducibility of transparent Ag_xO MESFET is less distinctive.

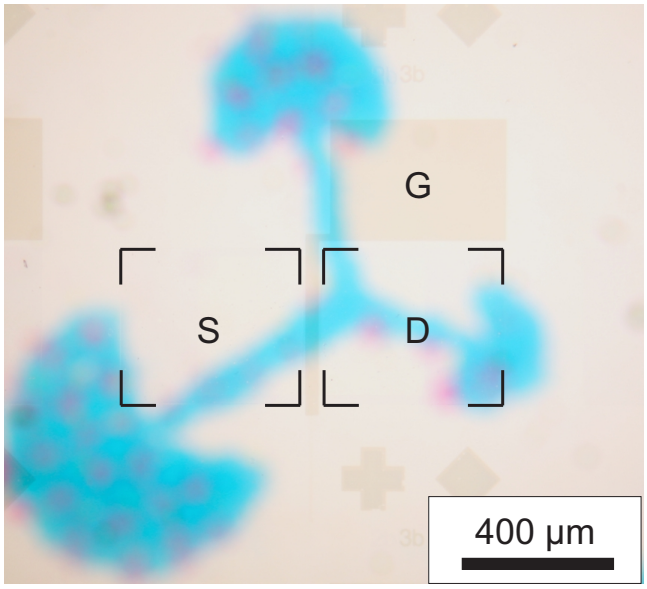


Figure 7.4: Microscopic image of a transparent MESFET. Background: printed logo of the graduate school "BuildMoNa" on a transparency. S: source, D: drain, G: gate. The corners of the S and D electrodes are marked with lines.

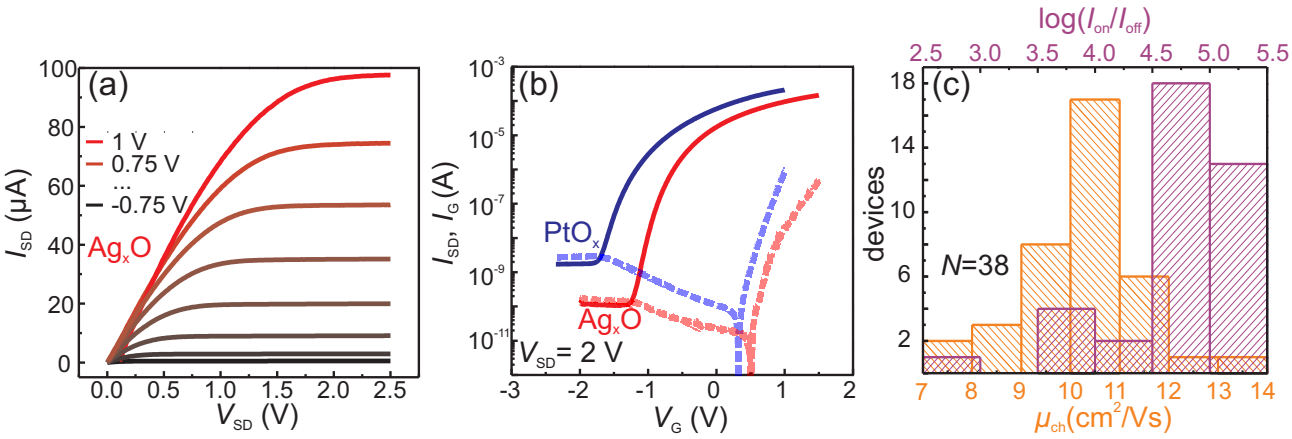


Figure 7.5: a) Output characteristic, b) Transfer characteristics and c) Reproducibility of transparent MESFET.

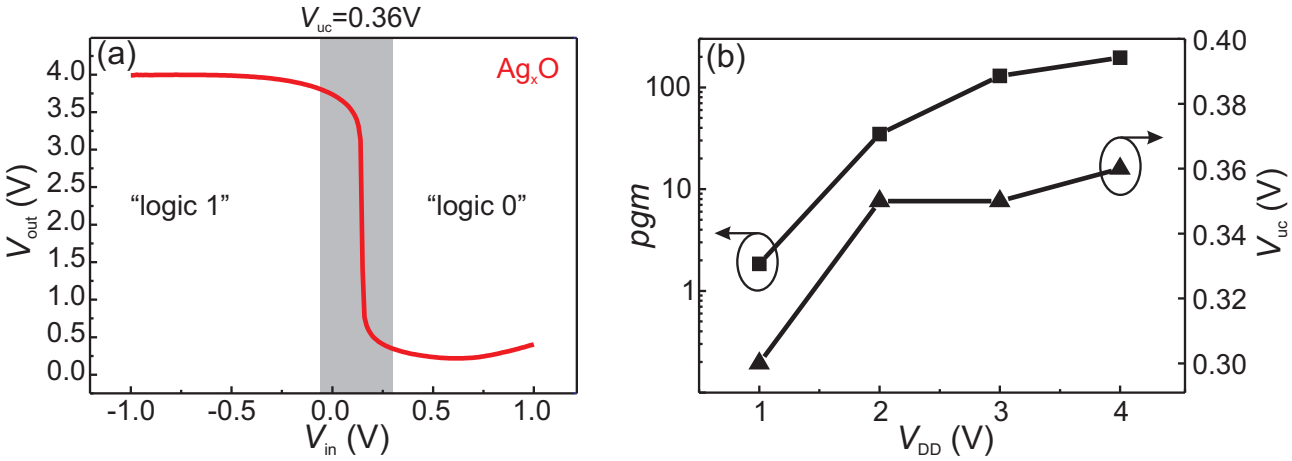


Figure 7.6: a) VTC, b) *pgm* and V_{uc} of a transparent MESFET inverter.

7.4 Transparent Inverters

On the basis of the above shown transparent MESFET, a fully transparent inverter is demonstrated. The presented device consists of the fundamental inverting part of the circuit shown in Sec. 6. In order to combine it with other devices (e.g. inverter chain acting as a ring oscillator) the criterion $V_{out} < V_{on}$ for the subsequent gate has to be fulfilled and a level shifter, e.g. FL or SDFL, has to be connected in series as described in the Secs. 6.2 and 6.3. With that, it is possible to create a complete transparent logic based on NOT (inverter)- and NOR-elements.

The inverter characteristic of a transparent Ag_xO-MESFET inverter is shown in Fig. 7.6a. For negative V_{in}, V_{OH} approaches V_{DD} whereas for positive V_{in} it is $V_{OL} \approx 0.2$ V. This value is higher than for the simple inverters in Sec. 6.1 due to leakage currents over the gate of the forward biased switching transistor. This can be optimized since it is not observed for opaque ZnO MESFET-based inverters (Cha. 6).

Figure 7.6b depicts the operating voltage dependence of *pgm* and V_{uc}. The *pgm* value increases drastically with V_{DD} and covers 2 orders of magnitude within a voltage range of 4 V. The maximum V_{DD} is limited to 4 V due to the increasing probability of breakdown of the load transistor Q_L. The uncertainty level V_{uc} shows a step from 0.3 V at $V_{DD} = 1$ V to 0.35 V at $V_{DD} = 2$ V and then remains constant. This is due to a shift of the inverter characteristic by 0.2 V towards positive V_{in} probably caused by a parasitic capacitance at the gate contact of Q_S.

7.5 Comparison with transparent devices from the literature

The device parameters of the transparent MESFET presented in this work are among the best reported for transparent transistors. Figure 7.7 shows a literature review of the channel mobility μ_{ch}, slope S, on/off-ratio and gate voltage sweep ΔV_G for the given on/off-ratio. The green box in Fig. 7.7a corresponds to the requirements on transparent electronics formulated by Wager [Wag03] for the on/off-ratio and channel mobility. For the sake of low power consumption, low electric fields and

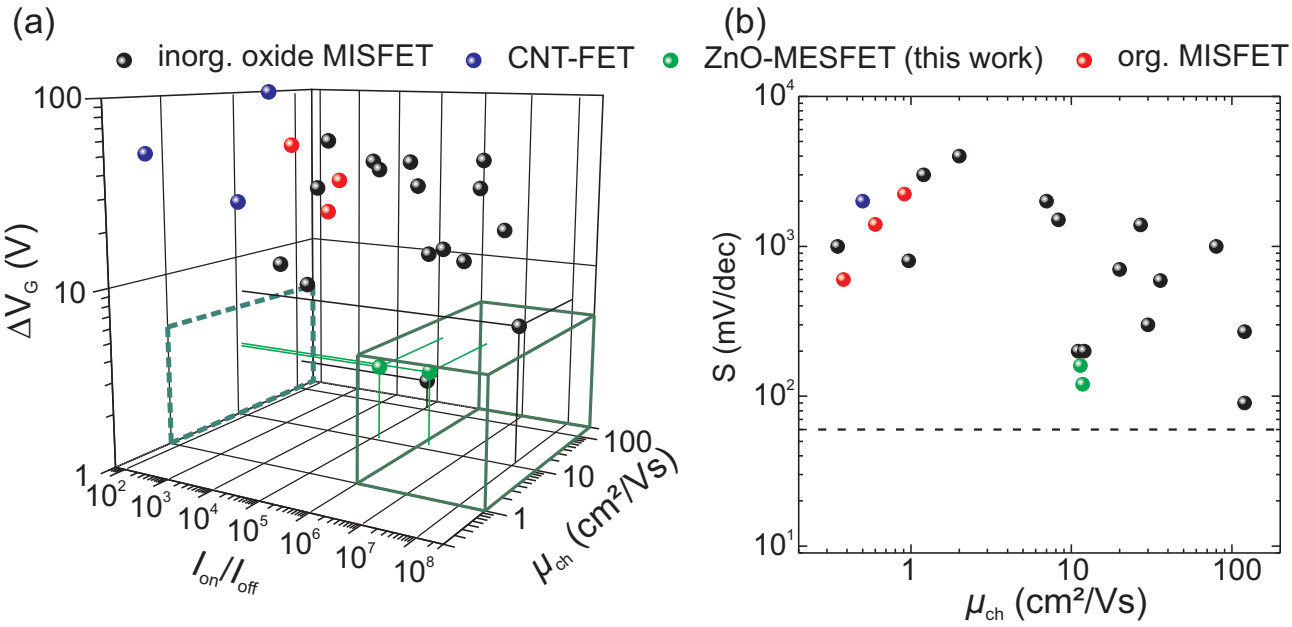


Figure 7.7: Comparison of parameters of transparent MESFET of this work with reported transistors.

therefore low crosstalk between individual devices in an integrated circuit, it is suggested to limit the gate voltage sweep (and with that the source-drain-voltage sweep) to the range below 5 V. With that, the ZnO-MESFET with Ag_xO gate in this thesis is the only FET which meets all of the requirements. There are three devices nearly fulfilling the requirements: two inorganic oxide MISFET [Yab06, Wan06] and the PtO_x-gated MESFET of this work. In Ref. [Yab06] Yabuta *et al.* reported a MISFET based on amorphous $InGaZnO_4$ as channel and Y_2O_3 as insulator. They reach the requirements in on/off-ratio (10^8) and mobility (12 cm^2/Vs) but the operating voltage still needs to be reduced. Wang *et al.* reported in Ref. [Wan06] a hybrid inorganic/organic bottom-gate MISFET with indium oxide as channel and an organic self-assembled superlattice dielectric having excellent characteristics (μ_{ch} = 120 cm^2/Vs, $\Delta V_G \sim 2$ V). However, their on/off ratio of 10^5 has to be improved by a factor of 10 and the organic dielectric can unfortunately not be processed by standard photolithography techniques. It is clear from Fig. 7.7a that organic and carbon-nanotube FETs are up to now not compatible with the requirements of transparent electronics. CNTs are hard to handle and exhibit low on/off-ratios. Although they can reach high channel-mobilities, their gate voltage sweep is too large. Organic FETs suffer from low channel mobility and on/off-ratio, and require high operating voltages.

The potentially achievable on/off-ratio of transparent ZnO-MESFET is not yet fully utilised. It can be improved for example by means of geometry and device design (e.g. higher W/L-ratios) as shown in Cha. 5. The advantages of ZnO-MESFET can also be seen in Fig. 7.7b, where the subthreshold slope is correlated with the channel mobility. Together with the FETs reported in Ref. [Wan06], ZnO MESFET approach the theoretical minimum slope of S = 60 meV (Eqn. 5.1) [Jit09, Lia91] for FETs operating at room temperature (dashed line in Fig. 7.7b). The slopes are S = 160 mV/decade and S = 120 mV/decade for PtO_x and Ag_xO, respectively. All other reported transparent FETs have much higher slopes which leads to long switching times of circuits based on them.

Within an inverter structure, the superior properties of the TRC are most evident. Among the transpar-

Table 7.2: Comparison of transparent inverter parameters.

channel	type	*pgm*	V_{rev} (V)	V_{uc} (V)	V_{DD} (V)	pgm/V_{DD} (1/V)	ref.
$Zn_{0.997}Mg_{0.003}O$	MESFET	196	0.2	0.36	4	49	this work
ZnO	MISFET	~ 5	~ 3	~ 2	10	0.5	[Sun08]
IGO	MISFET	1.5	~ 8	~ 12	30	0.05	[Pre06]
a-IGZO/pentacene	MISFET	56	2.84	~ 0.9	7	8	[Na08b]
ZTO	MISFET	10.6	~ 3.3	1.87	10	1.06	[Hei09]

ent inverters reported so far, the inverters based on ZnO-MESFET show an outstanding performance at a considerably low operating voltage V_{DD} = 4 V exhibiting the highest gain and the lowest uncertainty level (see Tab. 7.2).

With *pgm* = 196 (Fig. 7.6), the transparent inverter is ideally suited to be used as transparent voltage amplifier for low signal measurements. The performance of the inverters (V_{uc} = 0.36 V) is already comparable with the well established GaAs MESFET technology (V_{uc} ~ 0.1 V). The advantage of this MESFET-based inverter is obvious compared to the ZnO MISFET-based inverter reported in [Sun08]. There, *pgm* was in the range of 5 and V_{uc} > 2 V for V_{DD} = 10 V and only about 60% of V_{DD} was reached as high level. For MISFET most of the gate voltage drops over the insulator, which leads to higher operating voltages and lower gain of the devices.

8 Summary and outlook

PLD-grown insulators ZrO_2 and HfO_2 insulators as well as Al_2O_3–ZrO_2–Al_2O_3 and Al_2O_3–HfO_2–Al_2O_3 sandwich-layer insulators were investigated by means of current-voltage and capacitance-voltage measurements within metal-insulator-metal (MIM) and metal-insulator-semiconductor (MIS) structures. Although X-ray diffraction patterns of the insulators grown with different substrate heater powers revealed that the room-temperature-grown ZrO_2 and HfO_2 are amorphous, their insulating properties did not show a clear tendency with respect to the heater power. All insulators exhibit conduction for positive applied voltages. For the single layers, the statistically obtained relative frequency of insulating contacts at −1 V is around 30 to 60% for MIM and 70 to 80% for MIS capacitors, respectively, whereas at +1 V it is only 0 to 10% for MIM and 10 to 15% for MIS-structures. The sandwich-structure insulators exhibit more insulating contacts: 80 to 100% at −1 V and 60 to 80% at +1 V. The most probable conduction mechanisms are Schottky emission and Poole-Frenkel emission as revealed by temperature-dependent IV measurements, which indicates low importance of shunts and grain boundaries. The dielectric constants obtained from QSCV mesurements are found to be in good agreement with the literature values. For the higher-temperature-grown MIS-structures, the κ-values in the range of 30 for ZrO_2 and HfO_2 are even higher than other reported values ($\kappa \sim 20$–25). QSCV measurements also revealed that there is an excess of positive charges, i.e. metal ions, within the insulators, which may be responsible for the forward conduction. The trap charges density per unit energy at the insulator-semiconductor interface obtained from admittance measurements lay in a typical range of 10^{11}–$10^{12}\,cm^{-2}eV^{-1}$. Sandwich-insulators are found to be more suitable for the application in MISFET than single layers.

ZnO-MISFET A top-gate ZnO-MISFET with a 90 nm thick Al_2O_3–HfO_2–Al_2O_3 sandwich-insulator was fabricated by means of a lift-off technique using Au as sacrificial layer. The normally-on MISFET exhibit a turn-on voltage of −6 V and the source-drain current can be tuned over five orders of magnitude within a gate-voltage range of only 7 V. The minimum subthreshold slope of 300 mV/decade is among the best reported for ZnO-MISFET. However, the channel mobility of 1.9 cm^2/Vs is a factor of ten lower than the Hall-effect mobility, which can be attributed to scattering at interface-trap charges.
In the bottom-gate configuration, more than 800 nm Al_2O_3 were neceassary to reduce the leakage currents below 10^{-10} A at ±60 V. A comparison is made between *a*-plane and *r*-plane sapphire substrate. Both MISFET showed normally-on behavior with turn-on voltages of −40 V and −50 V for *a*-plane and *r*-plane, respectively. However, the on-current, on/off-ratio and channel mobility was higher for the *r*-plane MISFET due to its higher free-carrier concentration. The diffusion of dopants seems to be more likely for the ZnO-channel on *r*-plane substrate. Compared to the top-gate MISFET, the channel mobilities of the bottom-gate MISFET are lower (0.3 cm^2/Vs for *a*-plane and 0.5 cm^2/Vs for *r*-plane).

ZnO-MESFET on sapphire The presented ZnO-based MESFET showed outstanding electrical properties compared to MISFET. On the standard substrate for ZnO thin-film growth, sapphire, variations of all possible parameters according to the ZnO MESFET design, i.e. gate metal, channel thickness and doping, channel mobility, gate width-to-length ratio, have been investigated. A standard configuration was found using Ag_xO as gate on a nominally undoped 20 to 30 nm thick ZnO channel without buffer layer. With that, an on/off-ratio of 10^8 and a channel mobility $> 10\,cm^2$ Vs was achieved, which is tunable within a gate-voltage sweep of only 3 V. The minimum slope of ~ 80 mV/decade is already close to the thermodynamic limit of 60 mV/decade. The highest achieved channel mobility of those standard ZnO-MESFET was $\sim 27\,cm^2$/Vs. It was shown that the channel mobility of MESFET usually equals the Hall-effect mobility of the respective semiconductor. However, leakage and parasitic currents can lead to deviations of the mobilities. From the other tested gate materials (Pt, Pd and Au), only Pt has shown a comparable performance. The variation of the channel thickness and the use of MgO-buffer layer led to either a drastically reduced on/off-ratio or complete failure of the MESFET. Also the use of intentionally Al-doped ZnO channels did not show an improvement. The highest on-current of 15 mA and on/off ratio of 5×10^8 could be achieved using an interdigitated contact structure with a gate width-to-length-ratio of 700 making the MESFET suitable for applications as pixel-driver transistors for active-matrix LCD or OLED displays. An increase of the channel mobility up to $50\,cm^2$/Vs was achieved by the improvement of the crystal quality using homoepitaxially grown ZnO channels. However, this MESFET have shown insufficient saturation behavior due to parasitic currents that flow through the ZnO substrate. The principle of a MESFET with a quantum-well-channel structure has been shown. A two-dimensional electron gas formed within the MgZnO/ZnO/MgZnO quantum well at a gate voltage of 0.5 V. In the same voltage range, a peak-like increase of the channel transconductance, which is directly related to the channel mobility, was observed.
The reliability and degradation effects of the MESFET have been investigated by means of current-voltage measurements at elevated temperatures and under the exposure to visible light, bias stress measurements and long-term stability measurements. At elevated temperatures up to 150°C, the MESFET with Ag-gates showed the highest stability followed by Pt. In contrast to MISFET, bias stress measurements on the MESFET revealed that there is no influence of interface charges; i.e. under positive or negative gate-voltage stress over a period of 22 hours, no turn-on voltage shift has been observed. However, there is an influence of visible light on the off-current and the turn-on voltage, which is larger for blue and violet light than for red and green light. There was evidence of persistent photo conductivity after light exposure. Long-term stability measurements over a period of 300 days have shown that the higher initial mobility and on/off-ratio of MESFET with ZnO channel decreases by one fifth within the first 100 days and then remained constant. Using a small amount (0.25%) of Mg in MgZnO channels leads to smaller, but temporarily stable channel mobilities and on/off-ratios. It was also observed, that the reproducibility of MgZnO-MESFET was higher than for ZnO-MESFET.

ZnO-MESFET on glass For the sake of low-cost industrial applications, ZnO MESFET have been fabricated on glass substrates. The standard MESFET fabrication parameters were found to be: a ~ 30 nm thick ZnO:Al-channel using a target with 0.01% Al, a substrate temperature of 675°C and an oxygen partial pressure of 3×10^{-4} mbar. A comparison of MESFET on quartz glass and two

commercial borosilicate substrates showed a significant difference in the channel conductivity. The highest mobility of 1.3 cm^2/Vs and on/off-ratio of 4.7×10^5 could be achieved for quartz. The MESFET on borosilicates showed one and two decades lower channel mobility. All MESFET on glass were normally-off due to compensation by indiffusion of defects such as Li, Na, K, B from the substrate into the channel, which were detected by mass spectroscopy. A broad distribution of defects was observed by means of admittance spectroscopic measurements. Contrary to the MESFET on sapphire, a fast degradation of the electrical properties for MESFET on quartz glass has been observed already within a periode of 10 days. The absolute turn-on voltage, on/off-ratio and channel mobility decreased, whereas the gate's Schottky barrier height increased, which implies an alteration of the oxidation of the gate material. During bias stress measurements, a small turn-on voltage shift $\Delta V_G \sim 0.2$ V was observed under dark conditions, which is assigned to the reduction of an initially photogenerated charge at the gate/channel interface or benefited by the higher amount of structural defects in the channels on glass. Under permanent illumination, those charges were not observed during bias stress measurements.

ZnO-MESFET inverters Based on the ZnO-MESFET technology, integrated logic circuits were fabricated. Three types of inverters: simple inverter, FET-logic inverter and Schottky-diode FET-logic inverter adapted from GaAs technology, were investigated. With the simple inverter, consisting of two normally-on MESFET, the peak gain magnitude could be increased from 2.5 at 1 V operating voltage to 250 at 4 V, whereas the uncertainty level was in a range between 0.3 V and 0.33 V. Furthermore, the deviations of the real inverter characteristic from the ideal one were related to leakage currents and breakdown currents of the switching transistor for the high-output and low-output deviation, respectively. The positive switching-point deviation is probably due to charge trapping at the gate/channel-interface. The principle of a level shifter consisting of Schottky diodes and one additional MESFET at the output side (FET-logic) or input side of the inverter (Schottky-diode FET-logic) was demonstrated for the ZnO-MESFET inverters. For the FET-logic inverter without insulating crossover, the output-voltage could be shifted up to −1.2 V at a pull-down voltage of −1.5 V. The *pgm* and V_{uc} was in a range between 20 and 80 as well as 0.09 V and 0.13 V for $V_{DD} = 1$ V and $V_{DD} = 3$ V, respectively. The low uncertainty voltage is well comparable to established GaAs MESFET. By means of the Schottky-diode FET-logic inverter, the influence of the switching transistor's turn-on voltage on the voltage-transfer curve was investigated. For the lower negative turn-on voltage, the inverter achieved a peak gain magnitude of 197 and lower uncertainty level $V_{uc} = 0.13$ V at $V_{DD} = 3$ V compared to $pgm = 141$ and $V_{uc} = 0.37$ V. With the level shifter, the input voltage was shifted by up to 1.5 V using two Schottky diodes. Additionally, a NOR-gate was implemented using a third diode at the input of the inverter.

Transparent rectifying contacts For the realization of fully transparent ZnO-MESFET electronics, a patent-pending transparent rectifying contact was developed and demonstrated within Schottky diodes, MESFET and inverters. The contact consist of the ZnO-channel layer, an ultrathin (~ 10 nm) transparent Ag_xO or PtO_x layer and an equally thin highly conductive oxide or metal as capping layer. The achieved overall transparency of the complete device structure was 70% and 60% for Ag_xO and PtO_x, respectively. The Schottky diodes showed excellent rectifying behavior with an ideality factor of up to 1.47, a maximum barrier height of 0.87 V and the reverse leakage currents at −2 V were

as low as 10^{-6} A/cm^2. The fully transparent MESFET and inverters exhibit comparable electrical properties as the presented opaque devices. With an on/off-ratio of 1.4×10^6, a channel mobility of 12 cm^2/Vs and a maximum gate-voltage sweep of 3 V, the MESFET, are among the best reported transparent field-effect transistors of any kind. The here presented transparent inverters are superior to other reported transparent MISFET inverters. They exhibit a peak gain magnitude of ~ 200 and an uncertainty level of 0.36 V at the operating voltage of 4 V.

Outlook The opportunities of the used pulsed-laser deposition system regarding insulators and MISFET are limited. For further investigations on this field, the problem with the metal excess and the amorphous growth of insulators has to be solved. The stoichiometry of the insulators should be further investigated and controlled, e.g. using a plasma-assisted PLD. With that, it should be possible to fabricate ZnO-MISFET and ferroelectric MISFET with lower operating voltages, higher on/off-ratios and higher channel mobilities. The specific properties of ferroelectric heterostructures with ZnO is part of ongoing investigations .
Many advantages of ZnO MESFET compared to MISFET were presented within this thesis. It is therefore suggested to develop this alternative technology for transparent electronics further. There are still some issues to be considered. The reproducibility, reliability and long-time stability of the devices has to be improved. For that, investigations are going on. Due to the diffusion and compensation issues of Ag, Pt gates are more favored. MESFET on amorphous channels such as indium zinc oxide and gallium indium zinc oxide will be considered, which should lead to higher reproducability and higher mobilities of the MESFET on glass. In order to reduce degradation and improve stress stability, the use of passivation layers will be investigated and the devices will be stored and tested in different ambient atmospheres. Regarding MESFET device applications, the fabrication and investigation of ring oscillators will be pursued and the influence of interface defects will be further studied by time-dependent measurements. Transparent MESFET amplifiers will be appied, e.g., in the direct electrical measurements of the action potential of biological cells under simultaneous microscopic observation. Further, the applicability of transparent MESFET as pixel driver transistors in active-matrix displays will be studied.

Appendix A

Overview of photolithography templates

The Figs. A.1 to A.5 depict the photolithography templates for the devices in this thesis. Due to the transparency of the substrate and the ZnO-channel, the alignment of the templates at structures on the samples is difficult. Therefore, additional alignment masks were deposited as first lithography step. For the templates in Fig. A.1 and Fig. A.3, Au was dc-sputtered on two edges of the sample in an angle of 90°. On these edges, the crosses and diamonds were aligned in the next steps. For the other templates (Figs. A.2, A.4 and A.5), a common alignment template was designed, consisting of edges, crosses and diamonds on which the subsequent marks can be aligned. With that, the accuracy of alignment was 5 μm and less.

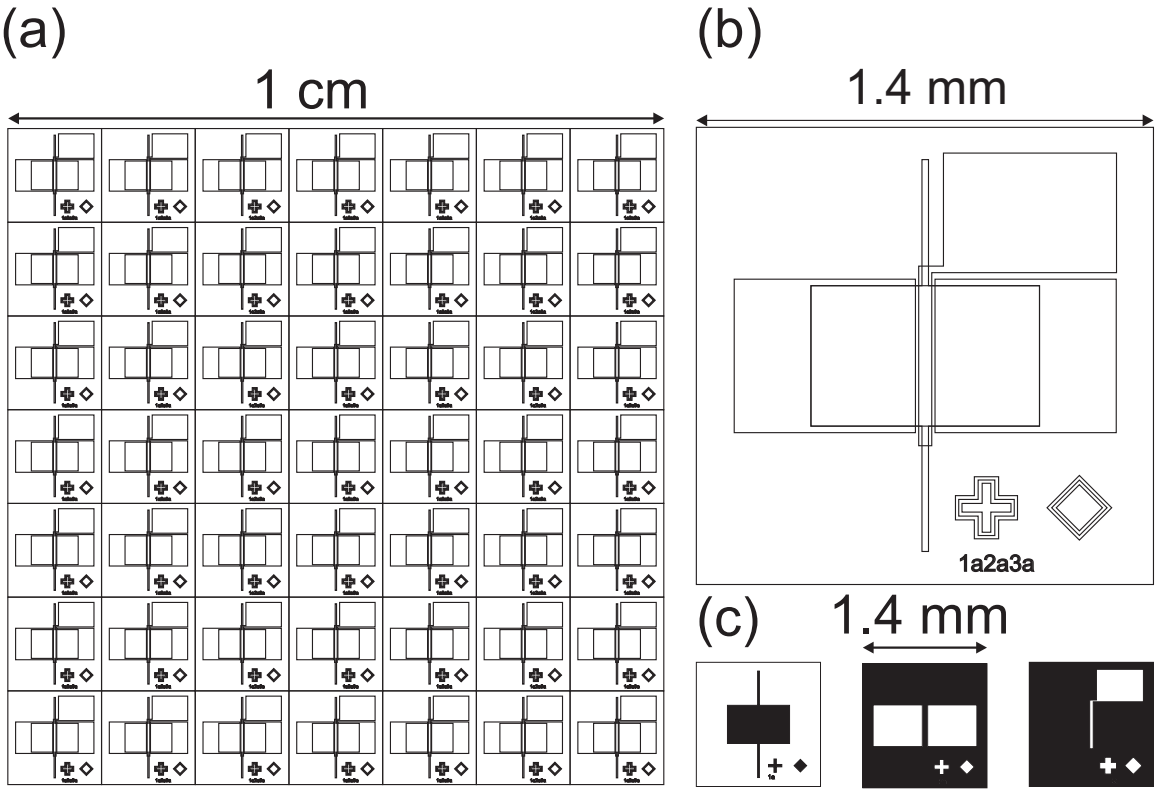


Figure A.1: Standard MESFET template. a) Overview of the 1×1 cm^2 sample with 7×7 transistors. b) Single FET with $W/L = 430\,\mu\text{m}/40\,\mu\text{m}$. The crosses and diamonds are alignment marks. c) Individual templates for the photolithography steps: mesa etching, source-drain contacts and gate contact. This template can also be used for MISFET fabrication.

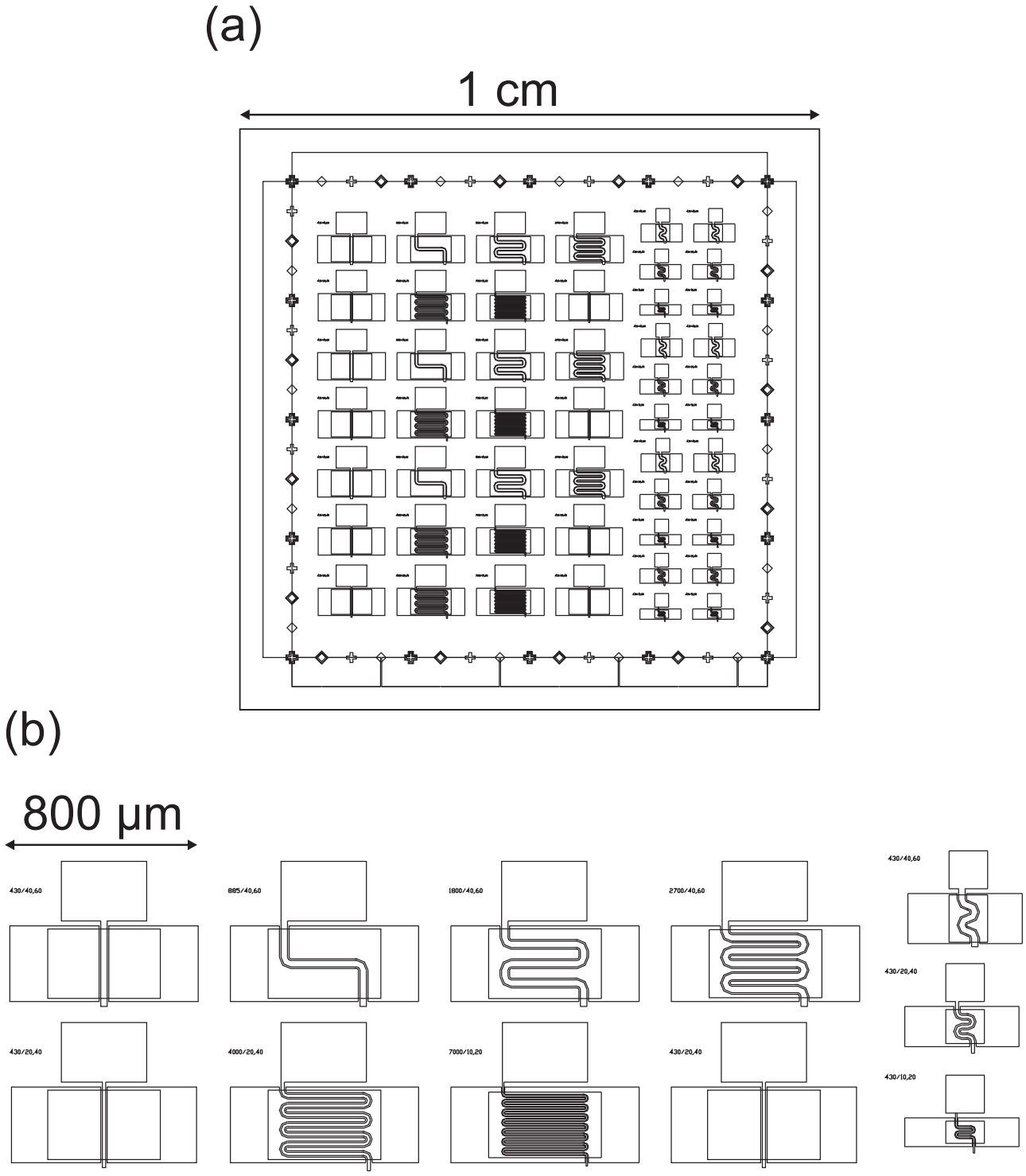


Figure A.2: Template for MESFET with interdigitated contact structure and miniaturization. a) Overview of the $1 \times 1\,\mathrm{cm}^2$ sample. b) Magnitifcation of the MESFET. Left: MESFET with various W/L-ratios on mesas with standard dimensions. Right: Miniaturized MESFET with standard W/L but on smaller mesas.

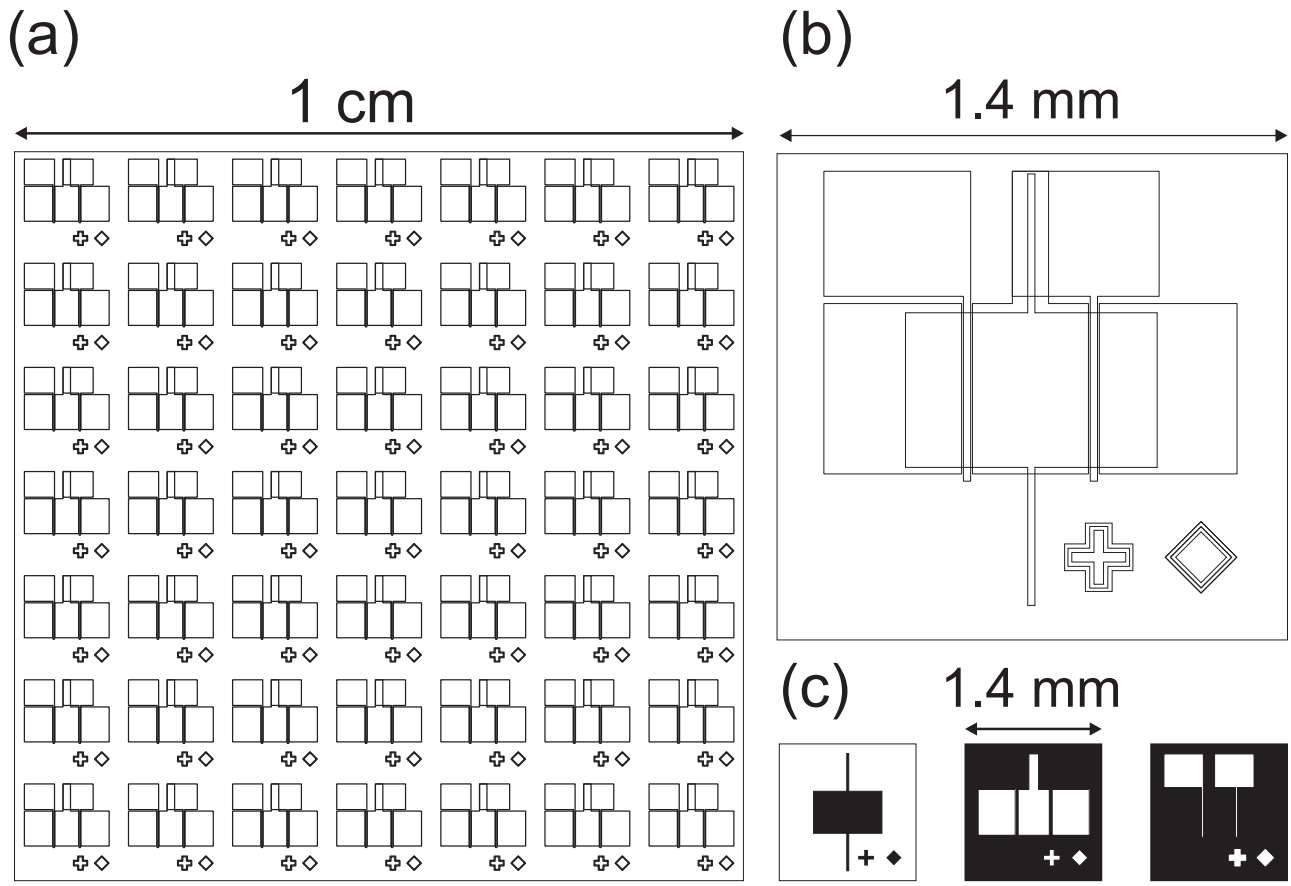


Figure A.3: Template for simple inverter. a) Overview of the $1 \times 1\,\mathrm{cm}^2$ sample with 7×7 inverters. b) Single simple inverter with the switching transistor and load transistor on a common mesa with standard dimensions. c) Individual templates for the photolithography steps: mesa etching, source-drain contacts and gate contacts.

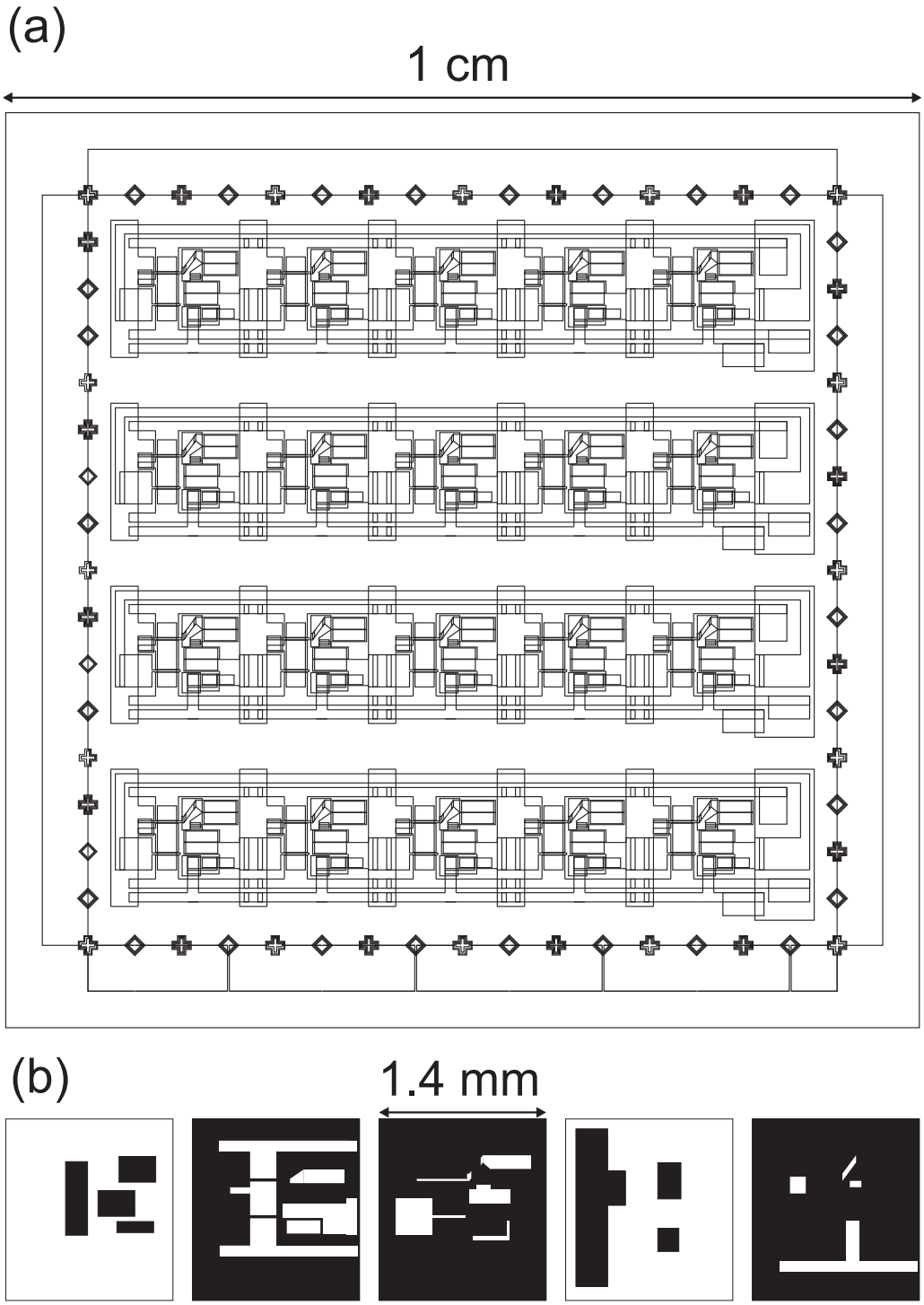


Figure A.4: Template for FL-inverter. a) Overview of the $1 \times 1\,cm^2$ sample with each 5 FL-inverter forming 4 5-stage ring oscillators. b) Individual templates for the photolithography steps: mesa etching, ohmic contacts, Schottky contacts, insulator, interconnections and crossover. For the FL-inverter without insulating crossover, the step before and after the insulator was merged.

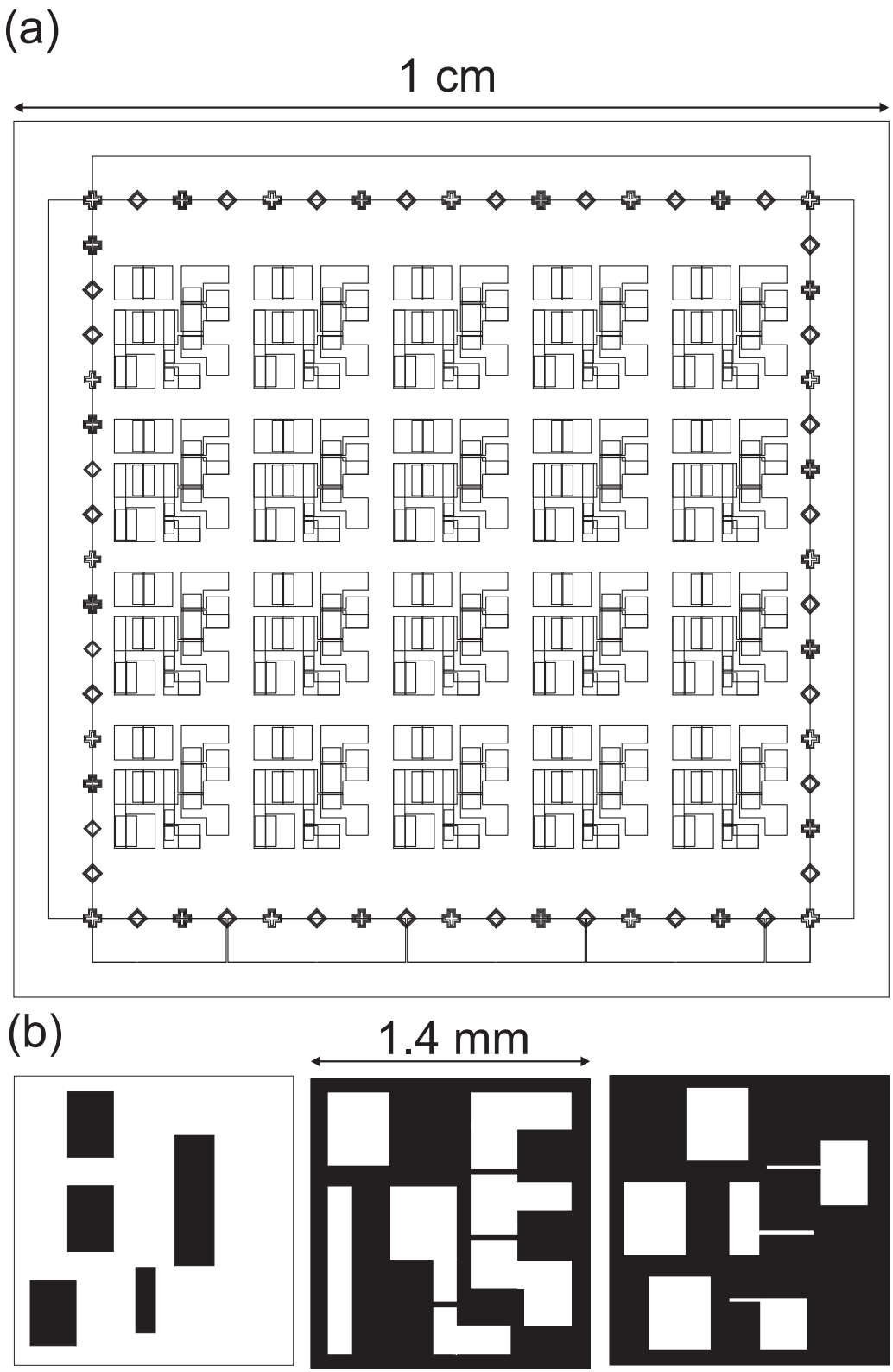


Figure A.5: Template for the SDFL-inverter. a) Overview of the $1 \times 1\,\mathrm{cm}^2$ sample with 5×4 inverters. b) Individual templates for the photolithography steps: mesa etching, ohmic contacts and Schottky contacts.

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Symbols and Abbreviations

χ_s ..... electron affinity of the semiconductor
ϵ_0 ..... vacuum dielectric constant
ϵ_i ..... insulator permittivity
ϵ_r ..... dielectric constant of the semiconductor
ϵ_s ..... permittivity of the semiconductor
η ..... ideality factor
κ ..... dielectric constant of the insulator
λ ..... wavelength
μ_{ch} ..... channel mobility
μ_n ..... electron mobility
ω ..... angular frequency
ϕ_B ..... Schottky barrier height
ϕ_m ..... work function of the metal
ϕ_n ..... energy difference between Fermi level and conduction band edge
ϕ_t ..... thermal potential
ψ_B ..... work function difference between Fermi energy level and intrinsic level
ψ_s ..... surface potential
ρ ..... space charge
τ_n ..... dcarrier lifetime
μ_{Hall} ..... Hall-effect mobility
A^* ..... Richardson constant
b_{min} ..... minimal resolution in photolithography
C ..... capacitance
C_D ..... depletion layer capacitance
C_{FB} ..... flat-band capacitance
C_i ..... insulator capacitance
d ..... channel thickness
$D(E)$ ..... density of states
D_{it} ..... interface trap charge density
d_{prox} ..... proximity distance
E_C ..... conduction band edge
E_F ..... Fermi energy level
E_g ..... energy band gap
E_i ..... intrinsic energy level
$f(E)$ ..... Fermi distribution
G ..... generation rate
g ..... inverter gain
g_{D0} ..... drain transconductance
$g_{m,sat}$ ..... saturation forward transconductance
g_{max} ..... maximum transconductance

h ..... Planck constant
$I_{SD,sat}$ ..... saturation current
I_{SD} ..... source-drain current
j ..... current density
J_{FN} ..... Fowler-Nordheim current
J_{ion} ..... ionic current
J_{Ohm} ..... Ohmic current
J_{PF} ..... Poole-Frenkel current
J_{SE} ..... Schottky emsission current
j_{sm} ..... current density from semiconductor to metal
j_s ..... saturation current density
k_B ..... Boltzmann constant
L ..... gate length
L_D ..... extrinsic Debye length
L_n ..... diffusion length
m^* ..... effective mass
n ..... electron concentration
N_A ..... concentration of acceptors
N_D ..... concentration of donors
N_f ..... concentration of fixed charges
n_i ..... intrinsic electron concentration
N_m ..... concentration of mobile charges
n_{n_0} ..... density of electrons at equilibrium
n_n ..... density of electrons in n-type semiconductor
n_s ..... surface density of electrons
NM_H ..... high noise margin
NM_L ..... low noise margin
P_D ..... power dissipation
p_{n_0} ..... density of holes at equilibrium
p_n ..... density of holes in p-type semiconductor
p_{O_2} ..... oxygen partial pressure
p_s ..... surface density of holes
pgm ..... peak gain magnitude
Q ..... charge
q ..... unit charge
Q_f ..... fixed charge
Q_{ind} ..... induced charge
Q_L ..... load transistor
Q_m ..... metal charge
Q_m ..... mobile charge
Q_{PD} ..... pull-down transistor
Q_p ..... inversion layer charge
Q_S ..... switching transistor
Q_s ..... surface charge
R_P ..... parrallel resistance
R_S ..... serial resistance
R_{rms} ..... root-mean-square roughness

S ..... subthreshold slope
s ..... resist thickness
S_{min} ..... minimal subthreshold slope
T ..... Temperature
T_S ..... substrate temperature
V ..... voltage
V_{bi} ..... built-in voltage
V_C ..... channel voltage
V_{DD} ..... inverter operation voltage
V_{ext} ..... external voltage
V_{FB} ..... flat-band voltage
V_G ..... gate voltage
V_{IH} ..... inverter input high level
V_{IL} ..... inverter input low level
V_{in} ..... inverter input voltage
V_i ..... voltage drop across insulator
V_{OH} ..... inverter output high level
V_{OL} ..... inverter output low level
V_{out} ..... inverter output voltage
V_P ..... pinch-off voltage
V_{rev} ..... inverter reversal voltage
$V_{SD,sat}$ ..... saturation voltage
V_{SD} ..... source-drain voltage
V_{SS} ..... pull-down transistor voltage
V_T ..... threshold/turn-on voltage
V_{uc} ..... uncertainty voltage range
v_x ..... charge velocity in x-direction
W ..... gate width
w ..... space charge region width
$\mathcal{E}$ ..... electric field
$\mathcal{E}_s$ ..... surface electric field
2DEG ..... 2-dimensional electron gas
AFM ..... atomic force microscopy
AHA ..... Al_2O_3–HfO_2–Al_2O_3
AMLCD ..... active-matrix liquid-crystal display
AMOLED ..... active-matrix organic light-emitting diode
AS ..... admittance spectroscopy
AZA ..... Al_2O_3–ZrO_2–Al_2O_3
AZO ..... aluminium-doped zinc oxide
BG ..... bottom-gate
CMOS ..... complementary metal-oxide-semiconductor
CV ..... capacitance voltage
DC ..... direct current
DLTS ..... deep-level transient spectroscopy
EDX ..... energy-dispersive X-ray spectroscopy
FEMFIB ..... field-emission microscope focused-ion beam
FFT ..... fast-Fourier transformation

FL ..... FET-logic
FN ..... Fowler-Nordheim tunneling
FWHM ..... full width at half maximum
GND ..... ground potential
HEMT ..... high-electron-mobility transistor
IC ..... integrated circuit
ITO ..... indium tin oxide
IV ..... current-voltage
IVT ..... temperature-dependent current-voltage
LBIC ..... light-beam induced current
LS ..... level shifter
MESFET ..... metal-semiconductor field-effect transistor
MIM ..... metal-insulator-metal
MIS ..... metal-insulator-semiconductor
MISFET ..... metal-insulator-semiconductor field-effect transistor
MOVPE ..... metal-organic vapor-phase epitaxy
NOR ..... not-or
PF ..... Poole-Frenkel emission
PLD ..... pulsed-laser deposition
QSCV ..... quasi-static capacitance-voltage
QW ..... quantum well
SDFL ..... Schottky-diode FET-logic
SE ..... Schottky emission
SEM ..... scanning electron microscopy
SI ..... simple inverter
SIMS-tof ..... secondary-ion mass spectroscopy time-of-flight
SNMS ..... secondary neutral mass spectroscopy
TCO ..... transparent conducting oxide
TE ..... transparent electronics
TEM ..... transmission electron microscopy
TFET ..... transparent field-effect transistor
TG ..... top-gate
TRC ..... transparent rectifying contact
TSO ..... transparent semiconducting oxide
VTC ..... voltage-transfer characteristic
XRD ..... X-ray diffraction
YSZ ..... yttria-stabilized zirconia

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